International Journal of Electronics Engineering (ISSN: 0973-7383)
Volume 10 • Issue 1 pp. 218-224 Jan 2018-June 2018 www.csjournals.com

Design of low power VCO based on current re-used topology in 0.13 µm CMOS

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Abstract: This paper stupendously demonstrates the modified current reused technique to design the low power VCOs. This paper also presents the proposed current re-used VCO and its three different topologies viz. traditional current re-used circuit, negative-resistance enhancement current re-used circuit, current-reused cross coupled VCO with DC level shifter and their comparison among them on the basis of low power consumption. The proposed chip is implemented in a 0.13 µm CMOS process. After comparing these topologies, it is found that proposed current re-used VCO circuit provides lower power consumption of 2.32 mW under the set supply voltage of 1.2 V as compared to other current re-used topologies. This topology also has good tuning range which exhibits better performance.
Keywords: Current-reused, Low power, Negative resistance enhancement, Voltage Controlled Oscillator (VCO).

Introduction

Voltage Controlled Oscillator is an electronic oscillator whose oscillation frequency is a linear function of controlled input voltage. Voltage Controlled Oscillator is of main importance in transceivers. To achieve good performance in transceivers, the three main key criteria of a Voltage Controlled Oscillator are low power consumption, low phase noise and good amplitude (1). Voltage Controlled Oscillators constitutes the very most important building blocks in communication systems (2). It is used for down-conversion and up-conversion in the transceiver as local oscillator. When it is designed in different CMOS technologies, the Voltage Controlled Oscillators is certainly a real solution in the radio frequencies of higher ranges due to its consumption in low power and lower values of phase noise in the market for wireless communication. LC-VCO is being widely used by the designers because of its consumption in lower power and lower phase noise specifications (3).

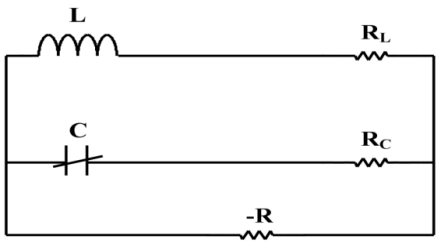

Fig.1. Conceptual diagram of LC VCO.

The fig.1 shows fundamental LC VCO circuit, in which inductor L is in parallel connection to capacitor C to form LC tank circuit. The oscillations are produced by the resonator tank circuit which is a loss of gtank. Where, gtank is the parallel combination of both inductor and capacitor resistances. To compensate these losses in a circuit, a negative resistance (-R), which is a negative conductance is added in a circuit. Since the negative conductance is produced by a active component i.e. -R, hence using this concept a LC VCO is designed by connecting both cross-coupled pair and tank circuit (4).

1.1. Key performance parameters of VCO

i. Center frequency: VCO which is being used in the environment determines the center frequency. For instance, uP clock generation network. Now a days as high as 10GHz frequencies are achieved by a CMOS VCOs (5).

ii. Tuning range: The two parameters which dictates the tuning range are (5):

a. VCO center frequency variations with process and temperature.

b. Necessity of frequency range for the application.

In designing the VCOs, the output phase and frequency variation is an important concern which results due to the noise on the control line. Hence in the output frequency, the noise is proportional to KVCO for any noise amplitude which is due to WOUT = WO + KVCO*VCONT . Here 'WO' is the intercept corresponding to VCONT = 0, 'KVCO' is the gain or sensitivity, 'VCONT' is the control voltage and

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'WOUT' is the output frequency. Hence VCO gain should be decreased to minimize the noise effect in VCONT.

iii. Tuning linearity: As the tuning characteristics are not linear in VCOs. Hence the settling behaviour of PLLs are degraded due to this non linearity. Therefore the variation of the gain is required to be minimized across the tuning range (5).

iv. Output amplitude: It is desired to get a large output amplitude waveform which is less sensitive to noise. There should be a trade off of amplitude among power dissipation, tuning range and supply voltage (5).

v. Power dissipation: Oscillators also suffers from trade off between power dissipation, noise, speed (5).

vi. Output signal purity: It may not be possible that the output waveform is not perfectly periodic if the control voltage is constant in a VCO. The output phase as well as the frequency can be corrupted by the electronic noise in the oscillator (5).

1.2. Complementary CMOS LC VCO

The two main advantages of complementary cross-coupled VCO as compared to that of cross coupled NMOS transistors topology are: Firstly the higher trans-conductance which is offered by the complementary topology with additional PMOS pair compensates for the loss in the circuit and consumes less current. Hence it is efficient in power consumption. Secondly, PMOS and NMOS transistors are matched, the symmetry properties provided by the complementary topology of the oscillating waveform are better and hence the up conversion of devices which have 1/f noise to the phase noise region of $1/f^3$ decreases (6). The complementary CMOS oscillator is shown in fig. 2. Oscillation starts to occur on satisfying the oscillation condition. As there is a growth of oscillation amplitude, the point is reached where there is not enough negative resistance which can support the loss of the LC tank if the maximum swing is not first clipped by the supply voltage and ground. Hence a point is reached where there is not increase in the further amplitude and the oscillations get stable (7). The phase noise performance of the complementary cross-coupled LC VCO is better if it is compared to that of only cross-coupled NMOS or PMOS oscillators keeping the same set of supply voltage as well as bias current in the limited current region (8). It is because of the larger maximum charge swing of complementary type cross-coupled LC VCO as compared to that of PMOS or NMOS cross-coupled oscillators only and this further enhances the performance of noise. There is another type complementary CMOS LC-VCO which is without tail and it shows better performance in phase noise as compared to that of the fixed biasing type (9).

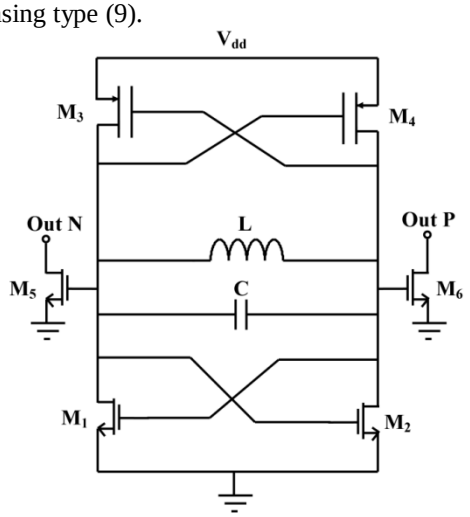

Fig.2 Complementary CMOS LC Oscillator (M5, M6 are buffers.)

The disadvantages of CMOS LC-VCO are:

1) Quality factor of the inductor is poor.
2) Limited tuning range of the varactor diodes.
3) Flicker noise is poorer in CMOS.

To eliminate these drawbacks, proposed current reused technique is studied in this paper. The rest of the paper is organised as follows: Current reused topologies have been studied in section 1.3. Section -II

describes the proposed current re-used VCO circuit. The comparison of the proposed low power VCO has been given in Results and Discussion section-III and section-IV concludes this paper.

1.3. Current re-used VCO topologies

In this paper, the topologies are studied on the basis of current-reused LC oscillator. The three current-reused topologies viz. Traditional current-reused circuit, Negative resistance enhancement current-reused circuit, DC level shifter VCO and the proposed current re-used VCO circuit are presented respectively (10).

i. Traditional current-reused circuit: It consists of LC tank circuit with CMOS circuit and hence the power consumption as well as the phase noise is reduced. But here due to passive components there is still a power dissipation which is not desirable. In this circuit, if the current which is to be drawn is reduced, then the power dissipation is also reduced by keeping the supply voltage constant. Its schematic diagram is shown in the fig.3 below. Here the inductor and the varactor diodes constitute the input conductance of the circuit. And this accounts for the LC tank circuit loss.

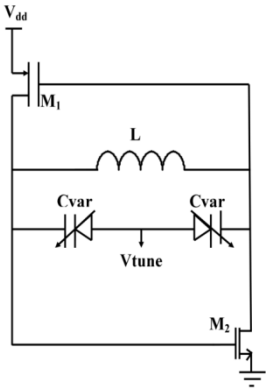

Fig.3 Traditional current-reused circuit.

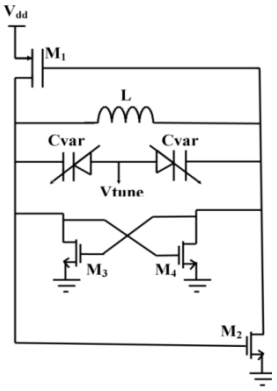

Fig.4 Negative resistance enhancement current reused circuit.

ii. Negative resistance enhancement current-reused VCO topology: In this topology, LC tank is connected with CMOS circuit along with extra pair of cross coupled NMOS are added. This extra pair of cross coupled NMOS further helps in compensating the loss due to the passive components in the circuit and acts as an negative resistance and further stabilizes the oscillator. Here in this topology the current drawn from the circuit is further reduced which further reduces the power dissipation keeping the supply voltage constant. Hence the negative resistance enhancement current-reused circuit needs less power as compared to traditional current-reused circuit. Its schematic diagram is shown in a fig.4. Similarly the inductor and the varactor diodes is the input conductance of the circuit which can be reduced with the help of additional cross coupled NMOS pair. The extra negative resistance produced by the NMOS pair is used to compensate the loss of the LC tank. Hence the oscillating condition achieved by the cross coupled extra NMOS pair makes it easier under same biased current.

iii. DC level shifter VCO topology: In this topology, a negative resistance enhancement current-reused circuit is used when dc level shifters are used in the circuit additionally. Here two MOS transistors, one PMOS and other NMOS are used with capacitors connected to both of them between drain and source terminals. This topology shows more symmetric output waveform as compared to other topologies without having dc level shifters applied to them. Hence if dc level shifters are used in the current reused topology on both NMOS and PMOS transistors, then the output waveform would be more symmetrical and further improves the noised performance. This topology is shown in the fig.5 given below.

Here in this topology, the capacitors used C1 and C2 are of high quality Q insulator metal which are used in parallel connection with additionally connected dc level shifters. These additional components reduce the effects of resistances and hence the noise problem is also improved.

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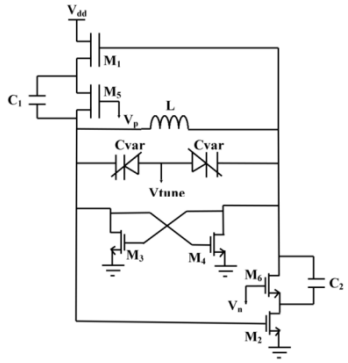
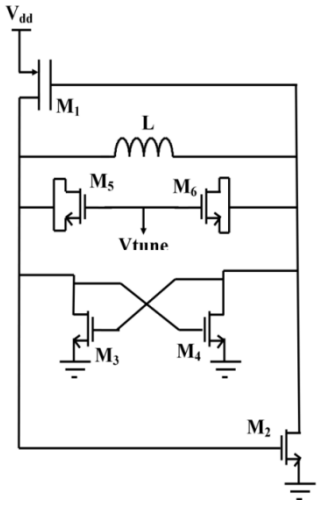


Fig.5. Schematic diagram DC level shifter VCO topology.

Proposed current re-used circuit topology

This VCO topology is also based on the current re-used technique except the fact that in this topology NMOS transistors are used in place of varactor diodes. NMOS transistors are working as same varactor diodes and provide the same tuning facility. In this topology, the source and drain of NMOS transistors which are used in place of varactor diodes are short circuited and hence displays the tuning property. The main idea to replace varactor diodes by NMOS transistors is because of the low power consumption and better immune to noise. The extra cross coupled NMOS pair acts as a negative resistance pair and provides extra negative resistance which compensate for the losses in the circuit. And it is found that, it draws a very small amout of current as compared to other topologies under same set of supply voltages. This current re-used VCO circuit topology is shown in a fig.6 below.

The negative resistance is produced by cross coupled pair also known as active pair is $-G_N$ and hence compensating for the losses in the circuit which is also known as passive loss i.e. G_P which is produced by passive elements(inductor and capacitor). This is shown in a fig. 7 which is a simple LC-VCO tank circuit. And the various parts of this circuit are also analyzed below.



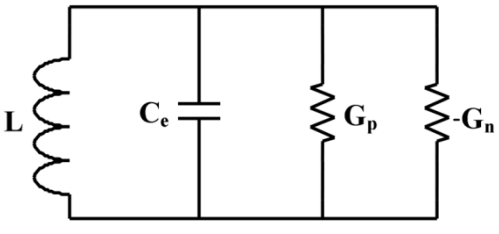


Fig.6. Proposed VCO circuit. Fig.7. Simple LC-VCO structure.

LC tank passive circuit: This LC tank circuit generally consists of varactor components and inductor component whose quality factor is usually high. The oscillator frequency is controlled by the proper selection of inductor and varactor model values. Where, G_P defines the loss in passive element of LC tank circuit (16).

LC tank active circuit: this active tank circuit provides the negative resistance ($-G_{N)}$ and hence compensating the circuit loss (16).

In fig.3, the input conductance which is G_{in1} is obtained by the equation given below (16):

$$G_{in1} = -(1/gmp_1 + 1/gmp_2^{-1}) \quad (1)$$

Now if G_P is the passive component LC tank loss, then the oscillation start-up condition is given by following (16):

$$G_P + G_{in1} \leq 0 \quad (2)$$

But in proposed current-reused VCO circuit, cross-coupled pair is connected additionally. Hence the reduced input conductance G_{in2} can be obtained by the same transistor sizes of M_3 and M_4 which is given as follows (16):

$$G_{in2} = -g_{mn3}/2 \quad (3)$$

Now the eq.(2) becomes is given by following (16):

$$G_P + (G_{in1} + G_{in2}) \leq 0 \quad (4)$$

The parameters which are used in our proposed current re-used VCO chip are shown in a table below.

Table 1 Device sizes.

	M_1	M_2	M_3	M_4	M_5	M_6
N_r	20	8	10	10	10	10
Lr(µm)	0.13	0.13	0.13	0.13	0.13	0.13
W_r(µm)	2	2	3	3	3	3
Type	PMOS	NMOS	NMOS	NMOS	NMOS	NMOS

The corresponding output waveform which is obtained when our proposed chip is implemented in a 0.13 µm standard CMOS process with inductor size of 1nm under the supply voltage of 1.2 V is shown in fig.8 below. The frequency tuning range is shown in fig. 9(a). The variation of power and frequency with supply voltage is shown in fig. 9(b).

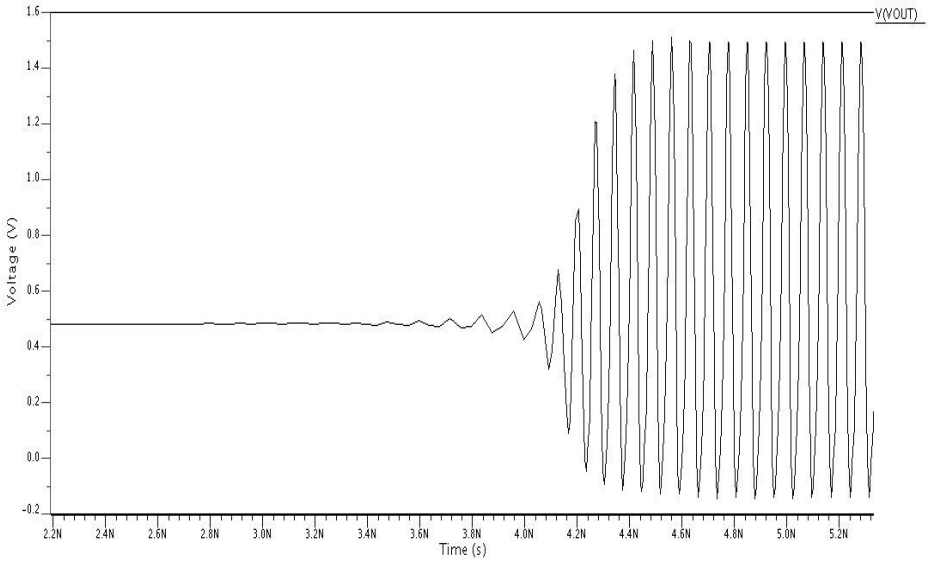


Fig.8 Output waveform when the supply voltage is 1.2 V.

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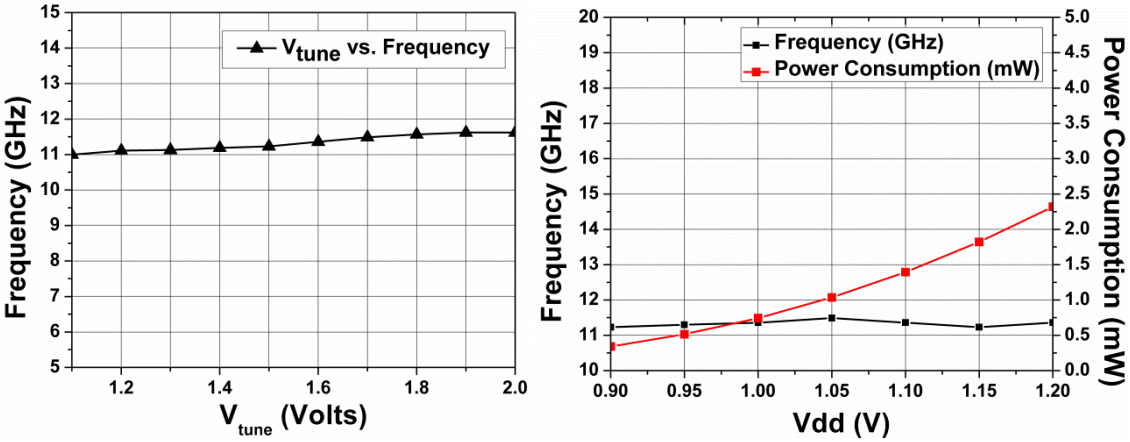

(a) (b)

Fig.9 (a) Frequency vs V_{tune} plot (b) Power consumption and frequency vs V_{dd} plot

Results and Discussions

The proposed current re-used VCO circuit is implemented in a 0.13um CMOS process under the supply voltage of 1.2 V which provides the power consumption as low as 2.32 mW with the tuning range between 11 GHz to 11.62 GHz. A comparison of previous work in current-reused VCOs with this work is done and is shown in the table given below. And it is seen from the comparison table that the proposed current-reused VCO topology has lower power dissipation. The frequency tuning range of proposed current-reused VCO topology is shown in fig.9.

Table 2 Comparison of VCO performance.

Reference	**(11)**	**(12)**	**(13)**	**(14)**	**(15)**	**(16)**		**This work**
Process(um)	0.13	0.18	0.13	0.13	0.18	0.18	0.18	0.13
Supply voltage (V)	0.8	1.8	1.2	1.8	1.5	1.5	1.5	1.2
Tuning range (GHz)	11.15 – 11.29	N/A	10.2 – 13	9.7 – 11.3	9.46 – 11.24	9.08 – 10.67	9.4 – 10.1	11 – 11.62
Frequency (GHz)	11.2	10	11.1	10	10.95	10.19	10.1	11.31
Power (mW)	4.8	7.2	26	14.4	5	3	2.88	2.32

Conclusion

The study is based on the comparison of three circuits on the basis of current re-used technology along with our proposed current re-used VCO circuit. The circuits which are studied viz. traditional current-reused circuit, negative resistance enhancement current-reused circuit, DC level shifter current-reused circuit and our proposed VCO circuit respectively. It is found that the second and third circuit shows considerable low power losses, though the third circuit namely DC level shifter current-reused circuit consumes a bit low power as compared to that of negative resistance enhancement current-reused circuit. But our proposed current-reused VCO circuit provides further low power dissipation as compared to that of DC level shifter VCO circuit. Hence it can be significantly concluded that the overall power consumption performance of our proposed current-reused VCO circuit is better and also exhibits good tuning range.

References

[1]. Moghavvemi, M. (2011). Performance Review of high quality factor low noise and wide band radio frequency LC-VCO for wireless communication. Microwave magazine, 130-146.

[2]. Cranincks Michiel, S. S. (1997). A 1.8 GHz low-phase noise CMOS VCO using optimized hollow spiral inductors. IEEJ Solid-state circuits 32(5).

[3]. Zhonglao Fu, A. P. (2007). Beating the power limits of LC Oscillations. Proceedings ofthe 50th Midewest symposium and circuits and systems , (pp. 441-444).

[4]. Ebrahimzadeh, M. (2011). Design of an Ultra Low Power Low Phase. International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering.

[5]. Razavi, B. (2001). Design of Analog CMOS Integrated Circuits. Singapore: McGraw-Hill.

[6]. B. De Muer, M. B. (2000). A 2-GHz low-phase noise integrated LC VCO set with flicker-noise upconversion minimization. IEEE Journal of solid-state circuits, 35, 1034-1038.

[7]. Lee, T. M. (2004). The design of CMOS Radio frequency integrated circuits (2nd ed.). Cambridge University Press.

[8]. Ali Haji-Miri, T. H. Lee (1999). Design issues in CMOS differential LC osciallations. IEEE Journal of Solid state circuits, 34, 717-724.

[9]. Roberto Alparicio, A. H. (n.d.). A Noise shifting differential Colpitts VCO. IEEE Journal of solid state circuits, 37, 1728-1736.

[10]. Seok-Ju Yun, S.-B. S.-C.-G. (2005). A mW current reuse CMOS differential LC-VCO with low phase noise. Digest of technical papers. Proceedings of the IEEE international conference on solid state circuits.

[11]. Yipping Han, L. E. (2006(18-20 Jan)). A low-voltage 12GHz VCO in 0.31 um CMOS for OFDM Applications . Proceedings of the topical meeting on Silicon Monolithic integrated Circuits in Rf systems . Digest of papers.

[12]. Zheng Gu, B. B.-G. (2003). Fully integrated 10GHz CMOS LC VCO. Proceedings of European Microwave conference, (pp. 583-586).

[13]. D. Axelrod, e. a. (2005). A multi-phase 10GHz VCO in CMOS/SOI for 40 Gbits

[14]. SONET OC768 clock and data recovery circuits. Proceedings of the symposioum on RFIC,(pp. 573-576).

[15]. S. Li, e. a. (2003). A 10GHz CMOS quadrature LC-VCO for multi-rate optical applications. IEEE J Solid state circuits , 1626-1634.

[16]. Meng-Ting Hsu, W.-J. L.-T. (2013). Design of low phase noise and low power modified current-reused VCO's for 10GHz applications. Microelectronics Journal, 44, 145-151.

[17]. Meng-Ting Hsu, C.-T. C. (2009). A low power 10GHz current reused VCO using negative resistance enhancement technique. Proceedings of the Asia Pacific Microwave conference (pp. 2276-2279). APMC.