International Journal of Electronics Engineering (ISSN: 0973-7383)
Volume 11 • Issue 1 pp. 618-621 Jan 2019-June 2019 www.csjournals.com

Coarse Grain Reconfigurable Multi-Core System for Image Edge Detection

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Abstract: In rapidly increasing demand for high performance and flexible hardware structure for an application, Multi-core systems are reaching its physical limits of complexity and speed. Coarse Grain Reconfigurable architecture provides flexibility in execution of application, uses less power and possesses fast processing speed. In this paper, Multi-core CGRA structure for an Image Edge detection technique is been proposed. This structure is blend of both Multi-core and CGRA. The results are tested and compared with the other CGRA structures.
Keywords: CGRA, Edge detection, Multi-core, Reconfigurable Architecture.

INTRODUCTION

In today's era, multi-core processing is a growing industry trend as single core processors rapidly reach the physical limits of possible complexity and speed. The need to realize higher performance while not driving up power consumption and heat has become a key concern. Hence a strong demand for high performance and flexible application is forcing designers to move to multi-core systems. Multi-core architectures give a brand new dimension to proportion the amount of process components (cores) and, therefore, the potential computing capacity [1]. But still this computational capability of multi-core system are questioned while executing computationally intense task. The hunger for high performance with low power consumption and flexibility in applications is never ending.
Recently, Coarse Grained Reconfigurable Architectures (CGRA) are developed to bridge the gap between power-hungry microprocessors and single-purpose ASICs. Coarse-grained arrays have the benefits of power-efficiency for their intended application domain, and also they are designed with efficient implementation of dynamic reconfiguration supported in hardware and in design software.Coarse-Grained Reconfigurable design (CGRA), with strong performance advantage as well as ability to be flexed post fabrication, is one such key building block. Recent design proposals, both academic and commercial, includes CGRAs for DSP applications or are completely based upon CGRAs. Since the normal application of FPGAs is usually restricted to prototyping and emulation, design methodology of CGRAs is still an emerging field. CGRAs in modern systems are getting clear and define roles with various design flows are being proposed. Regardless of the approach followed by these style flows, the central challenges of design remain same [2].
Since configuration codes are very short in dynamic reconfiguration, the execution can be very fast. But their use remains in question because of the dearth of a well-defined style flow and business convenience.

RELATED WORK

Till date many Reconfigurable Architectures have been proposed. Here in this paper we are discussing Edge detections techniques specific CGRA or reconfigurable structures. QUKU [3] is a mix of CGRA and FPGA. The aim is not only to achieve efficient dynamic reconfigurable system but also make it commercially available and affordable technology. Theapplication specificreconfiguration is obtained by operation of each PE, and the interconnections between PEs. The reconfiguration latency is reduced through maximum reuse of arithmetic and logical operators. PEs in QUKU is a heterogeneous array, with each PE optimized for just the range of operations it requires to implement for one application set.
A mesh topology based design of reconfigurable fabric(RF) to achieve parallel processing techniques is proposed in [2]. Reconfigurable Fabric contains set of homogeneous processing elements(PE) for 2 dimensional processing. This structure is tested using image edge detection technique for various system parameters like power, processing speed and area using various FPGAs. [2]

PROPOSED CGRA STRUCTURE

The proposed system consists of 8 homogeneous 16-bit Processing Elements P1 to P8 connected with shared bus as shown in fig 1. These Processing can be either any simple ALU or it could be even advanced processor. Here in this case PEs shown in fig.2 are specially designed cores with internal code and data memory as well as

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CPU which performs arithmetic and logical operations.CPU of PEs contains 16 bit ALU, Control unit, Instruction Decoder and 7 registers.

The main processor controllers the overall operations of pre-processed input image, storage of input image in one of the memory, managing of intermediate data and controls the scheduler which overall controls configuration of structure. Structure have 3 different memories 1) Configuration Memory 2) Data Input Memory and 3) Data Output Memory.

Configuration memory have customized instructions which configures each PE for applications. Here we are discussing Edge detection applications so configuration memory have instructions for each processing elements. This memory is managed through paging systems i.e. memory Page 0 is associated with P1 and so on. Same is applicable to other two memories.

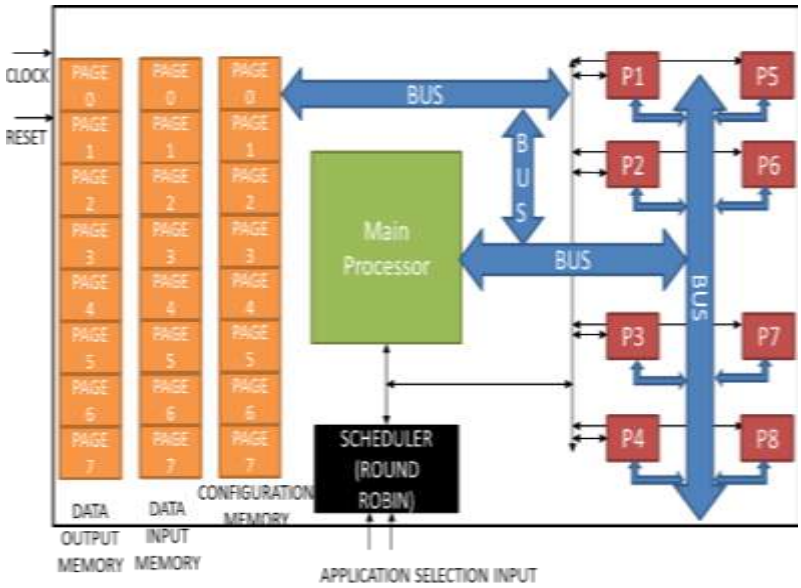

Fig. 1 Proposed Multi-Core CGRA Structure

Input data memory contains image data which is to be operated by Processing Elements from the respective pages. Output data memory is to store the final result of application. The scheduling of PEs is done by the scheduler in Round-Robin algorithm.

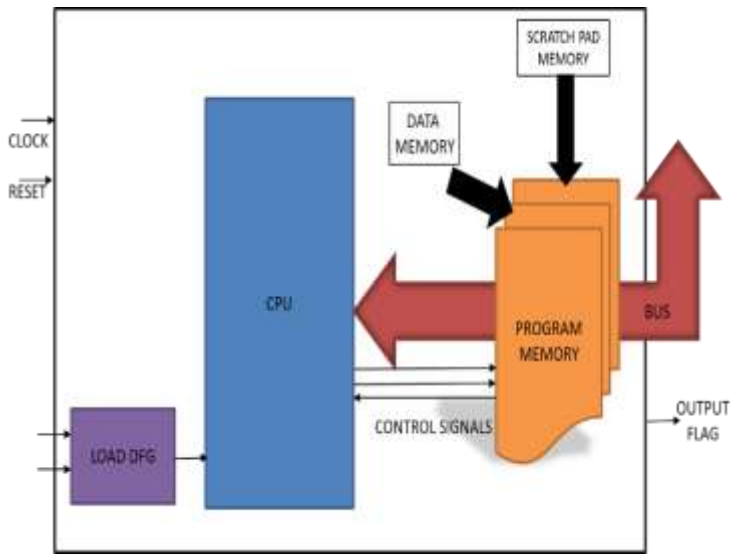

Fig. 2Structure of Processing Element / Core

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MAPPING AND EXECUTION OF IMAGE PROCESSING APPLICATION

In this section, the focus will be on edge detection algorithms that find widespread application in image processing. For applications like object detection, Edge detection is most commonly preferred. There are severaltechniques for edge detection. Many of them can be clustered into either Gradient or Laplacian. Gradient method concentrates on finding out minima or maxima in the first derivative while Laplacian method goes with zero crossings in the second derivative. On Proposed CGRA Structure, Sobel edge detection algorithms have been mapped.

The Sobel operator executes a 2-D spatial gradient measurement on an image and give emphasis to regions of high spatial gradient that correspond to edges. It is used to find the approximate absolute gradient magnitude at each point in an input greyscale image. The Sobelmasks are shown in Fig. 3. Sobel edge detector uses a pair of 3X3 convolution masks, one estimating the gradient in X direction and the other in Y direction. The approximate gradient magnitude is then obtained by adding the X and Y gradients. [3][4]

$$G(x)=\begin{bmatrix}-1 & 0 & 1\\ -2 & 0 & 2\\ -1 & 0 & 1\end{bmatrix} \qquad G(y)=\begin{bmatrix}1 & 2 & 1\\ 0 & 0 & 0\\ -1 & -2 & -1\end{bmatrix}$$

Fig. 3 Sobel 3X3 Masks

The intended edge detection application is mapped on target system by using special customized instruction. The format of customized instruction is given in fig. 4[5].

Instruction format is of 16-bit wide. Bits D15 to D13 are for the operations, D12 to D6 are for the scheduler or main processor to decide which PE to be allot the operation which is only come into picture when intermediate data is to be operated. Here inter-dependency of PEs is taken care-off by main processor through the scheduler and customized instructions. Bits D0 to D2 are to specify internal CPU register of respective PE which will act as a source for the specified operation and bits D3 to D5 specifies the destination register mean the result of the operation to be stored in specified CPU register.

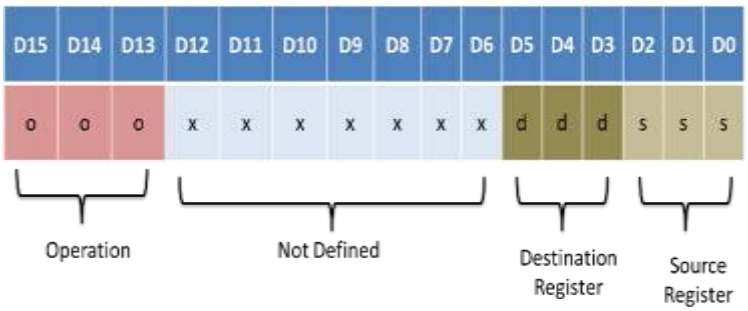

Fig. 4 Customized Instruction format

Edge detection algorithm is mapped as per the above mentioned format and stored in configuration memory. Input gray scale image in 256 x 256 format is to be pre-processed before storing in the memory

RESULT AND CONCLUSION

The images are processed in proposed structure and compared with other structures for same application give in Table1. It takes total 11.2 ms to complete edge detection of gray scale image of size 256 X 256 to process on proposed CGRA system with power consumption of 0.55 W.

TABLE I COMPARISON WITH DIFFERENT CGRA

Reconfigurable structure	Image Size (Row X Column)	Execution Time (ms)
QUKU[3]	336 X 341	54.4
Reconfigurable Fabric CGRA[2]	128 X 128	10.848
Proposed CGRA	**256 X 256**	**11.2**

The proposed multi-core CGRA systempreforms instructional levelparallel operations and requires less execution time. Reducing interdependencies between PEs and achieving Task level parallel execution will improve theexecution time, reconfiguration time and theoverall performance of the system. Proposed structure is best suitable forcomputationally intense operations and reduce overhead of loop operations. The same structure is useful for other signal/image/video processing applications.

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