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A Comparative Study of Aluminium Top Gate ZnO-Nanowire FETs with SAM Gate Dielectric

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Abstract: In this paper, the high-performance ZnO-nanowire FETs with patterned metal top-gate electrodes have been studied. A top-gate is developed that uses a very thin gate dielectric consisting only of an alkylphosphonic acid SAM that can be deposited from solution. The insulating quality of the SAM is investigated for top-gate FETs that utilize aluminium for the top-gate electrode. The comparison between aluminium top-gate ZnO nanowire FETs with aluminium oxide as dielectric and aluminium top-gate ZnO nanowire FETs with SAM dielectric is studied. When aluminium is used for the top-gate electrode, a hybrid dielectric is formed at the interface between the SAM and the aluminum, consisting of the SAM and a spontaneously formed aluminium oxide layer. The hybrid gate dielectric of the aluminium top-gate FETs was found to have a total thickness of 5-11nm. Owing to the hybrid gate dielectric, the aluminium top-gate FETs are operated with gate currents below 1pA for voltages up to 3V. The low gate current makes it possible to apply larger overdrive voltages compared to the gold top-gate FETs and therefore the aluminium top-gate FETs show larger drain current and larger transconductance. An aluminium top-gate FET with a peak transconductance of 50µS, an on/off current ratio of 10^8, and a subthreshold slope of 100mV/decade has been demonstrated.

Keywords: Nanowire, field-effect transistor, zinc oxide, aluminium oxide, SAM.

1. INTRODUCTION

Over the past two decades the field of semiconductor nanowires has been one of the most active areas of research, with an exponentially increasing number of publications, more than 5500 publications in 2010 [1]. The growing interest is accompanied by an increasing number of techniques to manufacture nanowires from much different semiconductor material, such as silicon, gallium arsenide or zinc oxide to name just a few. In general, these fabrication techniques can be divided into two different categories, the top-down approach and the bottom-up approach. In the top-down approach, high-resolution patterning techniques, such as electron-beam lithography [2], stencil-mask lithography [3], nano-imprint lithography [4] or super lattice nanowire pattern transfer [5], are utilized to define quasi-one-dimensional nanowires by etching from three-dimensional bulk semiconductors or by metal evaporation. In contrast, the bottom-up approach relies on the assembly of atomic or molecular building blocks to build up the desired nanostructures. The potential of the bottom-up approach is the possibility to control the growth of nanostructures with near-atomic precision and to fabricate nanomaterials with distinct chemical composition and structure, which may not be accessible with conventional top-down fabrication methods [6, 7]. Common bottom-up techniques for the synthesis of nanowires are vapor-liquid-solid growth [8, 9], vapor-solid growth [10], or wet-chemical growth [11]. Due to substantial progress in the control of nanowire synthesis, it is now possible to grow nanowires with controlled diameters and lengths [12], radial and axial nanowire heterostructures [13], and even nanowires with controlled kinks [14]. The high level of control of the nanowire growth and the unique properties emerging from the quasi-one-dimensional structure of the nanowires has opened many novel applications for nanowires. To give an example, the group of Charles Lieber at Harvard University recently demonstrated the recording of electrical signals from the inside of a living cell using a specifically tailored V-shaped silicon nanowire [15].

The more traditional field for the potential application of nanowires is their use as active components in field-effect transistors (FETs) in future integrated circuits, such as microprocessors and non-volatile memories. The small dimensions of nanowires are promising for the realization of novel device geometries, such as gate-all around FETs [16] or vertical FETs [17, 18]. Compared to planar devices, the nanowire geometry is expected to provide better current control and allow for higher integration densities [19].

Besides the use in high-integration-density applications, semiconducting nanowires are also potentially useful in realizing high-performance FETs in large-area electronics, such as active-matrix displays [20] or sensor arrays, which require less complex circuitry and smaller FET densities. In state-of-the-art active-matrix displays thin-film transistors (TFTs) based on hydrogenated amorphous silicon or polycrystalline silicon are usually utilized to control the individual pixels. However, the processing of these materials typically requires temperatures above 300°C, which prevents their use on unconventional substrates, such as plastics or paper. Flexible polymeric substrates usually have a glass transition temperature below 200°C, so that semiconductors

that can be processed at lower temperatures are required for the fabrication of large-area electronics on flexible substrates. Materials that are potentially useful for the fabrication of FETs on flexible substrates are organic semiconductors [21], amorphous metal-oxides [22] and also single crystalline nanowires [23]. Although the synthesis of single crystalline nanowires often requires temperatures above 200°C, the nanowires can be grown on a substrate that can tolerate these high temperatures and then be transferred to the target substrate for FET assembly. As long as the temperature during FET manufacturing is below the glass transition temperature of the substrate, FETs based on semiconducting nanowires can be realized on polymeric substrates. Compared to TFTs based on organic semiconductors and amorphous metal-oxides, the larger charge-carrier mobilities of single-crystalline nanowires make it possible to reduce the lateral dimensions of the FETs while providing the same current. This is especially beneficial for display applications, since the area consumption of the FET restricts the size of the pixel emitter and hence reduces the aperture ratio.

The aim of this paper is the development of high-performance, low-voltage, top-gate FETs based on single-crystalline ZnO nanowires that can be fabricated at low temperatures and can thus be implemented on flexible substrates. Gate dielectrics based on SAMs are popular in the field of organic electronics and have shown low defect density, excellent insulating properties and large capacitances. However, their use for FETs based on inorganic semiconductors is much less investigated.

2. INTERFACIAL ALUMINIUM OXIDE AS A GATE DIELECTRIC FOR ALUMINIUM TOP-GATE FETS

The use of aluminium as the gate metal for top-gate ZnO-nanowire FETs is investigated. Two different gate dielectrics are utilized. The insulating properties of the interfacial aluminium oxide layer that forms spontaneously at the interface between the oxygen-plasma-treated ZnO nanowire and the aluminium top gate are examined. Subsequently, the use of a SAM gate dielectric with an aluminium top-gate electrode is also investigated. It has been shown that an insulating interfacial aluminium oxide layer is formed at the interface between ZnO and aluminium, when the ZnO nanowire is exposed to an O_2 plasma immediately prior to the aluminium deposition. In the following it is investigated whether the ability to tune the ZnO/Al interface from ohmic (Ar-plasma treatment) to insulating (O_2-plasma treatment) permits the fabrication of top-gate ZnO-nanowire FETs which utilize the interfacial aluminium oxide layer as the gate dielectric.
To prepare ZnO-nanowires FET with interfacial aluminium oxide gate dielectric, ZnO nanowires are dispersed on a Si/SiO_2 substrate and annealed at 600°C. The source and drain contacts are fabricated by EBL, Ar-plasma treatment, and thermal evaporation of 80nm thick aluminium. Next, the top gate is defined in the center of the nanowire by EBL, oxygen-plasma treatment (30sccm O_2, 10mTorr, 50W, 15sec), and aluminium evaporation (O_2-contact). A schematic of the FET is shown in figure 1 (a). In order to allow time for the formation of the interfacial aluminium oxide layer, the devices are characterized after two days of storage in ambient air. Since the FETs are realized on a Si/SiO_2 substrate, the charge-carrier concentration in the ZnO nanowire can be modulated either by the global silicon back gate or by the local aluminium top gate.

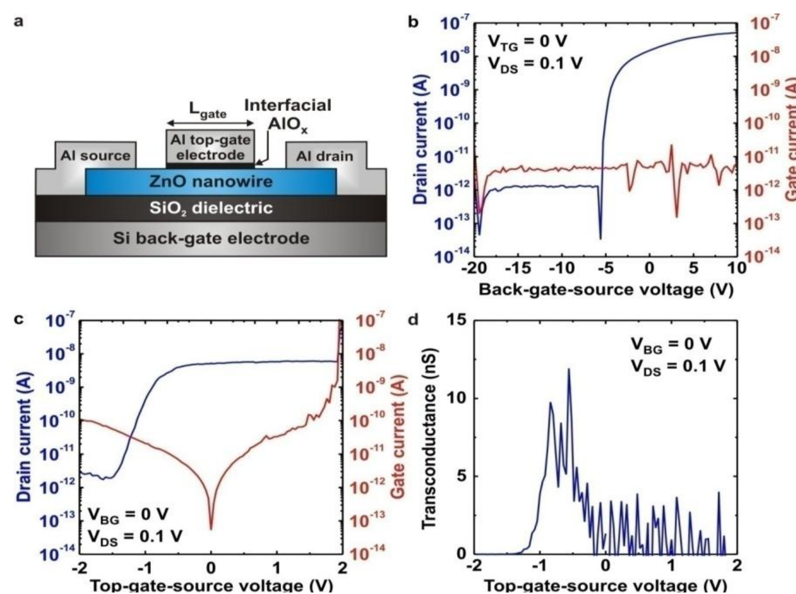

Figure 1: ZnO-nanowire FET in a dual-gate configuration with a global back gate and a non-overlapping Al top gate.

Figure 1 (a) shows schematic device structure of a dual-gate ZnO-nanowire FET (L= 3µm, d_{NW}=40nm, t_{SiO2}=100nm). The conductivity of the ZnO nanowire can be modulated either by the global back gate or by the local top gate. The gate dielectric for the top gate consists of the thin aluminium oxide layer that forms spontaneously at the interface between the O_2-plasma-treated ZnO and the deposited Al top gate. Figure 1 (b) shows back-gate transfer characteristics for V_{DS}=0.1V and a top-gate voltage V_{TG} =0V. Figure 1 (c) shows Top-gate transfer characteristics for V_{DS}= 0.1V and a back-gate voltage V_{BG}=0V. The gate current increases symmetrically, as expected for charge carriers tunneling through a thin barrier. At V_{TG} = 2V the gate dielectric breaks down. Figure 1 (d) shows transconductance as a function of the top-gate voltage. Due to the fact that the top gate does not overlap the source and drain contacts, the transconductance is near zero for V_{TG}>0V.

Figure 1 (b) also shows the transfer characteristics of a dual-gate ZnO-nanowire FET obtained by sweeping the back-gate voltage (V_{BG}) from -20V to 10V. The drain-source voltage is 0.1V and the top-gate voltage (V_{TG}) is 0V. The FET has a channel length L=3µm and the nanowire diameter is d_{NW}= 40nm. The gate current is shown in red. Figure 1 (c) shows the transfer characteristics of the same device when the drain current is modulated by sweeping the top-gate voltage V_{TG} (V_{DS} = 0.1 V and V_{BG} = 0 V). Because the interfacial aluminium oxide top-gate dielectric is thinner and has a larger capacitance than the SiO_2 back-gate dielectric, the voltage necessary to modulate thecharge-carrier concentration is much smaller (V_{TG} = ±2 V). Again, the gate current is plotted in red. In contrast to the gold top-gate devices presented in section 8.2.1, the top gate does not overlap the source and drain contacts. Therefore, the gate current shown in figure 1 (c) is a measure of the leakage current through the interfacial aluminium oxide layer at the interface between the O_2-plasma-treated ZnO nanowire and the aluminium top gate.

2.1 GATE-CURRENT ANALYSIS

The behavior of the gate current can be well understood by figure 1 (b) and 1 (c). The thin interfacial aluminium oxide layer acts as a tunnel barrier. For top-gate voltages V_{TG} between -1V and 1V, the gate current shows a symmetric increase around 0V as expected for current limited by tunneling For larger V_{TG}, the gate-current increase becomes asymmetric. While for V_{TG}<1V, the slope of the gate current slightly decreases, the gate current starts to fluctuate for V_{TG}>1V and finally the gate dielectric breaks down at V_{TG}~2V. The asymmetry of the gate current in this regime indicates the presence of a Schottky barrier connected in series to the tunnel junction. For increasingly negative V_{TG}, the depletion width in the ZnO increases and V_{TG} drops across the depleted part of the ZnO nanowire and the interfacial aluminium oxide. For increasingly positive V_{TG}, the depletion width in the ZnO nanowire is reduced. Hence, the voltage drop across the interfacial aluminium oxide increases and approaches the breakdown voltage. As a consequence of the breakdown of the dielectric, the use of the top-gate FETs with interfacial aluminium oxide gate dielectric is limited to relatively small gate-source voltages between -2V to 1V.

2.2 TRANSCONDUCTANCE ANALYSIS

A gate electrode that only partially overlaps the semiconductor channel along a length L_{Gate} is unfavorable since this requires additional electrostatic or chemical doping of the channel areas not controlled by the gate. This becomes apparent when the relationship between the transconductance and the top-gate voltage is considered (see figure 1 (d)). For positive top-gate-source voltages the transconductance drops to near to zero. This is due to the fact that parts of the nanowire channel are not controlled by the gate, so that increasing the gate bias beyond 0V does not lead to a larger drain current. This clearly shows the necessity of a gate electrode that overlaps the S/D contacts and thus controls the entire channel. In summary, the spontaneous formation of an AlO_x layer at the interface between ZnO nanowire and Al top gate can be exploited to fabricate top-gate ZnO-nanowire FETs. However, the low quality of the interfacial aluminium oxide and the need for a gate electrode overlapping the entire nanowire channel and the S/D contacts limit the applicability of the interfacial aluminium oxide as a gate dielectric.

3. ALUMINIUM TOP-GATE ZnO-NANOWIRE FETs WITH SAM GATE DIELECTRIC

It has been shown that the gate current of an gold top-gate ZnO-nanowire FET can be significantly reduced when the ZnO nanowire is covered with a SAM that acts as a gate dielectric layer. Based on these results, the influence of a SAM on the gate currents of aluminium top-gate FETs is investigated. Since the insulating SAM based on alkylphosphonic acid molecules covers the ZnO nanowire and also the aluminium S/D contacts, the use of the SAM permits the gate electrode to overlap the S/D contacts.

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3.1 INVESTIGATION OF AL/ALO$_X$/SAM/AL LEAKAGE CURRENT

In order to quantify the insulating properties of the SAM in the regions where the Al gate electrode and the plasma-oxidized Al S/D contacts overlap, leakage-current-test junctions are fabricated with the help of polyimide shadow masks. Figure 2 (a) shows a photograph and a schematic cross section of the test junctions. The test junctions consist of an 80nm thick, O_2-plasma-oxidized aluminium bottom electrode, coated with a SAM based on pentadecylfluoro-octadecylphosphonic acid (FC_{18}-SAM, see inset figure 2 (b), and an 80nm thick aluminium top electrode. The test-junction area is 60µm x 60µm. The thickness of the plasma-grown aluminium oxide is expected to be around 3-4nm [104]. Figure 2 (b) shows the current density through 14 leakage-test junctions (blue curves, $Al/AlO_x/FC_{18}$-SAM/Al) as a function of the applied voltage. For comparison, the red curve shows the leakage current density of a test junction without FC_{18}-SAM, in which the dielectric layer consists only of the plasma-grown aluminium oxide ($Al/AlO_x/Al$).

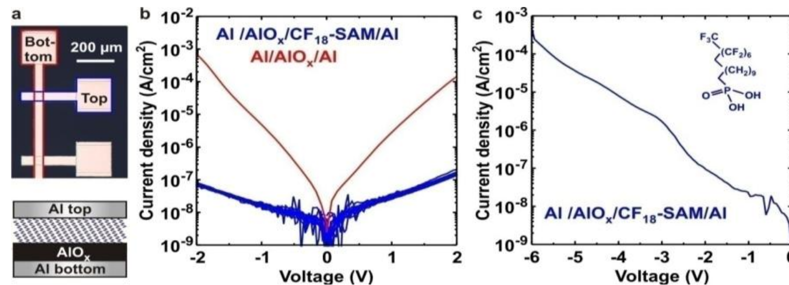

Figure 2: Leakage current density through $Al/AlO_x/FC_{18}$-SAM/Al junctions.

Figure 2 (a) shows Optical microscopy image and schematic cross section of the leakage-current-test junctions. The $Al/AlO_x/FC_{18}$-SAM/Al junction is defined in the overlap areas between the metal bottom electrode (framed red) and the metal top electrodes (framed blue). Figure 2 (b) shows Leakage current density through 14 $Al/AlO_x/FC_{18}$-SAM/Al junctions (blue curves). The insignificant variation of the leakage current confirms the junction uniformity. The red curve corresponds to the leakage current density of similar test junctions without FC_{18}-SAM. The FC_{18}-SAM reduces the leakage current density by more than three orders of magnitude. Figure 10.7 (c) shows Leakage current density through an $Al/AlO_x/FC_{18}$-SAM/Al junction under application of higher voltages. Up to -6V, the junction shows no indication of a dielectric breakdown.

The addition of the SAM leads to a reduction of the current density by more than three orders of magnitude at a voltage of 2V. The fact that the current fluctuations observed for the 14 $Al/AlO_x/FC_{18}$-SAM/Al junctions are extremely small indicates that the junctions are very uniform. Figure 2 (c) shows the leakage current density through an $Al/AlO_x/FC_{18}$-SAM/Al junction for voltages between 0V and -6V. This voltage range corresponds to the voltage drops observed across the overlap areas in the FETs. Up to a voltage of -6V the junctions show no indication of a dielectric breakdown.

3.2 ELECTRICAL CHARACTERISTICS OF ALUMINIUM TOP-GATE ZnO-NANOWIRE FETs WITH SAM GATE DIELECTRIC

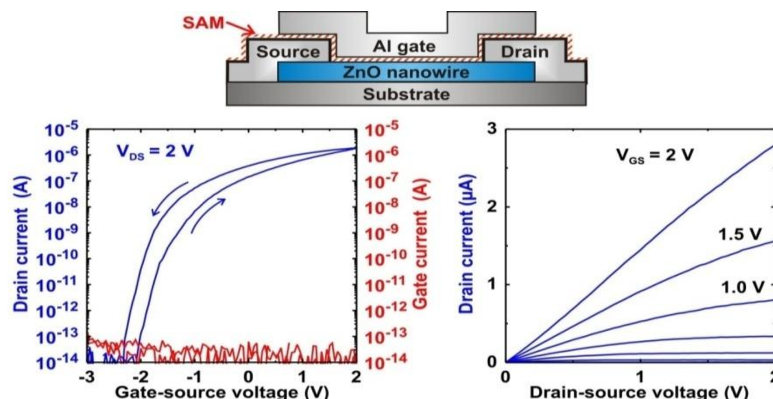

Figure 3: Transfer and output characteristics of an aluminium top-gate ZnO-nanowire FET with SAM gate dielectric.

The FET has a channel length of 1.5µm and the nanowire diameter is 60nm. From the transfer characteristics a transconductance of 1µS, an on/off drain current ratio of 10^7, and a subthreshold slope of 120mV/decade are

extracted. The small current leakage and the large breakdown voltage of the $Al/AlO_x/FC_{18}$-SAM dielectric with Al top electrode suggests that aluminium top-gate ZnO-nanowire FETs with gate electrodes overlapping the entire SAM-covered semiconductor channel and theSAM-covered aluminium S/D contacts can be fabricated with good yield and performance.

Figure 3 shows the transfer and output characteristics of an aluminium top-gate FET with SAM gate dielectric (L=1.5µm, d_{NW}=60nm). The FET has a transconductance of 1µS, an on/off ratio of 107, a subthreshold slope of 120mV/decade, and a small hysteresis of 0.4V. It is especially gate-source voltages. For V_{GS}<0V, the gate-current is expected to be small in accordance with the below 0.1pA up to a gate-source voltage of 2V. This is in contrast to the observations of the gold top-gate FETs and is especially surprising with regard to the expected lower height of the Schottky barrier between aluminium and ZnO. For a lower Schottky barrier height, the leakage current is expected to be dominated by the tunneling current, as has been previously observed for the top-gate FETs with interfacial aluminium oxide gate dielectric. However, the gate current of the aluminium top-gate FETs with SAM gate dielectric is more than four orders of magnitude lower than the gate current of the top-gate FETs with interfacial aluminium oxide gate dielectric for V_{GS}= 2V.

4. CONCLUSIONS

When aluminium is used for the top-gate electrode on the SAM-covered ZnO nanowires, it has been demonstrated that the gate dielectric consists of the SAM and an additional layer of aluminium oxide that spontaneously forms at the interface between the aluminium top-gate electrode and the SAM-covered ZnO nanowire. The formation of the aluminium oxide layer indicates that atmospheric oxygen difuses to the SAM/Al interface. It is believed that due to a poor surface-wetting of the aluminium on the SAM-covered ZnO nanowire, hollow regions have been formed at the SAM/Al interface which may lead to the diffusion of oxygen to the SAM/Al interface and thereby promote the formation of the aluminium oxide. The hybrid gate dielectric of the aluminium top-gate FETs was found to have a total thickness of 5-11nm. As a result, the aluminium top-gate FETs operate with gate currents below 1pA for voltages up to 3V. The low gate current makes it possible to apply larger overdrive voltages compared to the gold top-gate FETs and therefore the aluminium top-gate FETs show larger drain current and larger transconductance. An aluminium top-gate FET with a peak transconductance of 50µS, an on/off current ratio of 10^8, and a subthreshold slope of 100mV/decade has been demonstrated.

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