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Design & Analysis of Two Stage CMOS Operational Amplifier for Low Power Design

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Abstract: Operational amplifiers are widely used and versatile electronics device and in this proposed work a two stage OpAmp is simulated utilizing 90nm technology on an EDA tool called Cadence Virtuoso. The purpose of purposed work is to develop a 2-stage CMOS OpAmp for low power with greater stability and to examine how different components affect its design characteristics. Voltage Gain for amplification, Phase Margin for stability, Unity Gain Frequency and Power Dissipation are the primary parameters that proposed amplifier aims to improve. A differential amplifier with a current mirror active load and a common-source amplifier make up the two stages of OpAmp.

Keyword: 2-stage CMOS operational amplifier, gain, unity gain frequency, phase margin and power dissipation.

1. INTRODUCTION

Fundamentally, an amplifier is a device that increases input signal strength and is intended to be operated in combination with external feedback elements between its output and input terminals, such as resistors and capacitors [1]. The general term "amplifier" is used to describe a circuit that produces a more powerful version of its input signal. Due to its capacity to amplify a relatively weak input signal, small signal amplifiers are frequently used devices. The operational amplifier studied, often known as an OpAmp, is a high-gain electronic voltage amplifier with differential input and that mostly has a single-ended output. The main goal of operational amplifier is to provide better amplification along with less power dissipation with higher bandwidth and greater phase margin for stability of amplifier [2-6]. With the right choice of the components and their values, the OpAmp can be used as a current to voltage converter, active rectifier, integrator, comparators, voltage follower, Differentiators, summing amplifier. Ideally an OpAmp should have infinite input resistance, infinity voltage gain, and zero output resistance [7]. However, after simulation the practical values will be discussed.

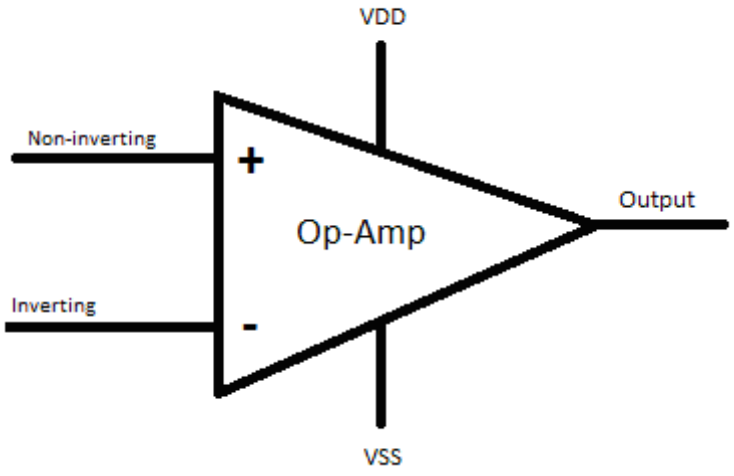

Figure 1: Symbol of OpAmp.

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As shown in figure 1, an op-amp contains five terminals: inverting input, the output, non-inverting input, negative power supply (VSS or often grounded) and positive power supply (VDD). One of the inputs is Inverting Input and it is recognized by a "minus" (–) sign. The other input named as the Non-inverting Input and is indicated by a "plus" sign (+). The third terminal of OpAmp is its output terminal and it can be a current or voltage [8].

2. DESIGN PROCEDURE

The 2-stage CMOS operational amplifier shown in figure 2 consists of two stages one is Differential-input single-ended output stage with PMOS current mirror as active load, the differential amplifier have two inputs that is V_{in+} and V_{in-} as first stage and second one is a common-source amplifier output stage to provide more voltage gain because gain provided by first stage is not sufficient and to provide low output resistance common-source amplifier is used.

The schematic of two-stage operational amplifier design as shown in figure 2 contains of a NMOS differential amplifier (MOSFET M_1 and M_2) with active load PMOS current mirror (MOSFET M_3 and M_4) as the first stage next comes the second stage, which is made up of PMOS (MOSFET M_6) and is common-source amplifier where mosfet M_6 works as an amplifier and mosfet M_7 works as the current source for biasing. Mosfet M_5 and M_8 form a NMOS current mirror and are used to bias the circuit to provide proper current and voltages to the circuit.

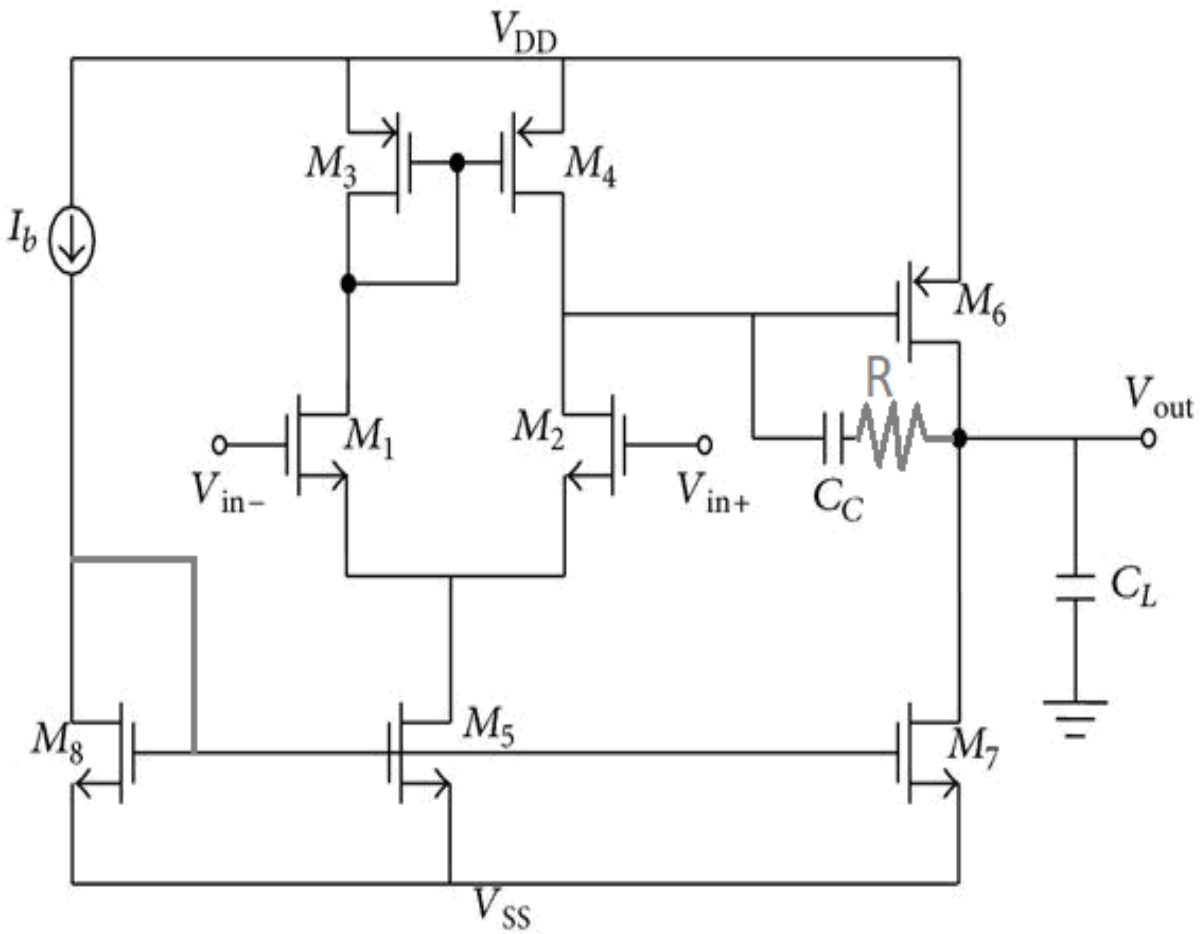

Figure 2: Two stage CMOS operational amplifier circuit diagram.

A feedback capacitor Cc that is connected between the second stage amplifier's input (or called as the first stage amplifier's output) and the second stage amplifier's output is used as a miller capacitance to obtain pole splitting (increasing the distance between the first and second pole) and that will provide better stability, along with capacitor Cc a resistor R that is called as nulling resistor and is connected to provide greater phase margin to achieve greater stability.

With the nulling resistor, we can move the RHP (right half plane) zero to infinity and a second option to achieve greater stability is to select R in a way that shifts RHP zero into the LHP (left half plane) such that it can be cancelled with one of the poles. However in this simulation we have chosen resistor R such that the RHP zero moves towards infinity or practically we can say towards a very higher frequency.

To achieve enhanced performance the values given to all the components of op-amp should be precise in a way that amplifier can achieve better gain, unity gain frequency, power dissipation and phase margin.

Table 1: Different components and their values.

Components	Values
V_{DD}	1.2 V
R	3.4 kΩ
C_C	4.5 pF
C_L	10 pF
V_{in}^+	DC= 1 Volt : AC= -1 Volt
V_{in}^-	DC= 1 Volt : AC= 1 Volt
V_{SS}	0 Volt

Table 2: Width and Length of all the MOSFET

Mosfet's	Practical values (W)	Practical values (L)
M_1, M_2	11µ	1µ
M_3, M_4	10µ	1µ
M_5. M_8	8µ	1µ
M_6	50µ	1µ
M_7	20µ	1µ

The width (W) and length (L) of all the mosfet's are described in table 2. Width and Length of mosfet is an important component of mosfet as by selecting the values of W and L in such a way that we can achieve greater gain, bandwidth and phase margin. The total width of mosfet M_3 and M_4 is 10µ (WP=10 µ) but the fingers for these mosfet are 5. Similarly total width of mosfet M_6 is 50µ (WPS=50 µ) but the fingers for this mosfet are 2.

3. SIMULATION OF PROPOSED DESIGN

Make the connections as shown in the figure 3. Insert the values of components and mosfet parameters (W and L) as described in table 1 and 2 respectively. The two-stage operational amplifier used a compensation technique called as Miller compensation.

Prior to the unity gain frequency, the system behaved like a single pole system. OpAmp's are stabilized using this compensation method by connecting a capacitance Cc and resistor R in a negative-feedback configuration across one of the internal gain stages, usually the second stage.

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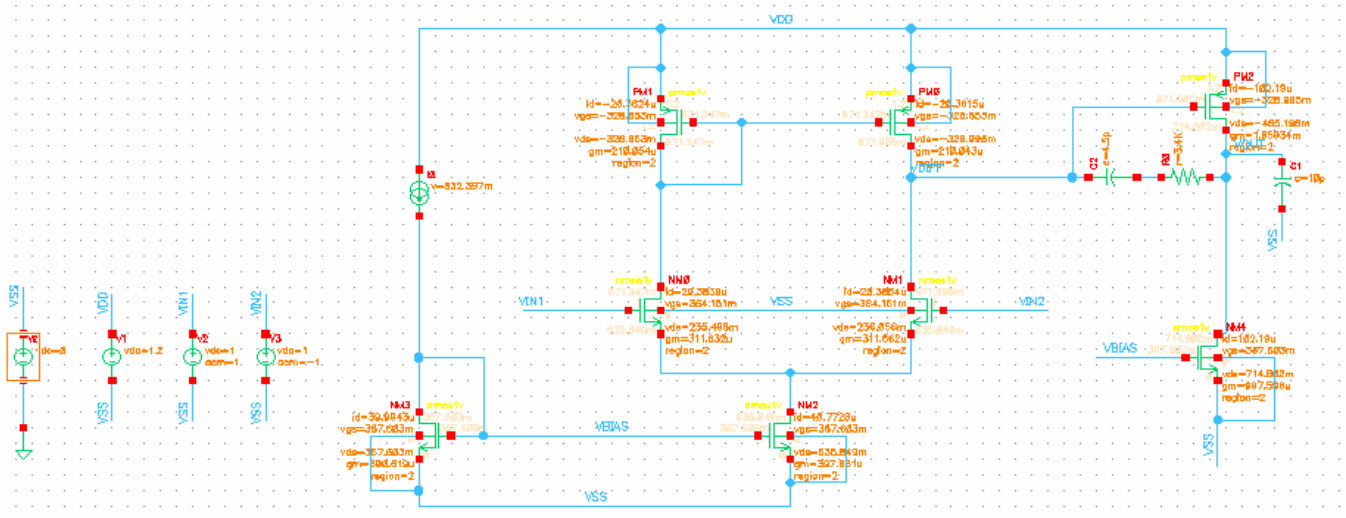

Figure 3: Two-stage CMOS operational amplifier Schematic.

4. Results and Discussion

The results of AC and DC simulations and a discussion for the suggested two-stage operational amplifier are presented in this section. With 90nm technology, the OpAmp is simulated and examined using the cadence virtuoso EDA tool. A broad range of frequencies were covered. The gain of the OpAmp is not constant in the open loop design and fluctuates with frequency. The product of gain and frequency remains constant up until the gain bandwidth product of the OpAmp.

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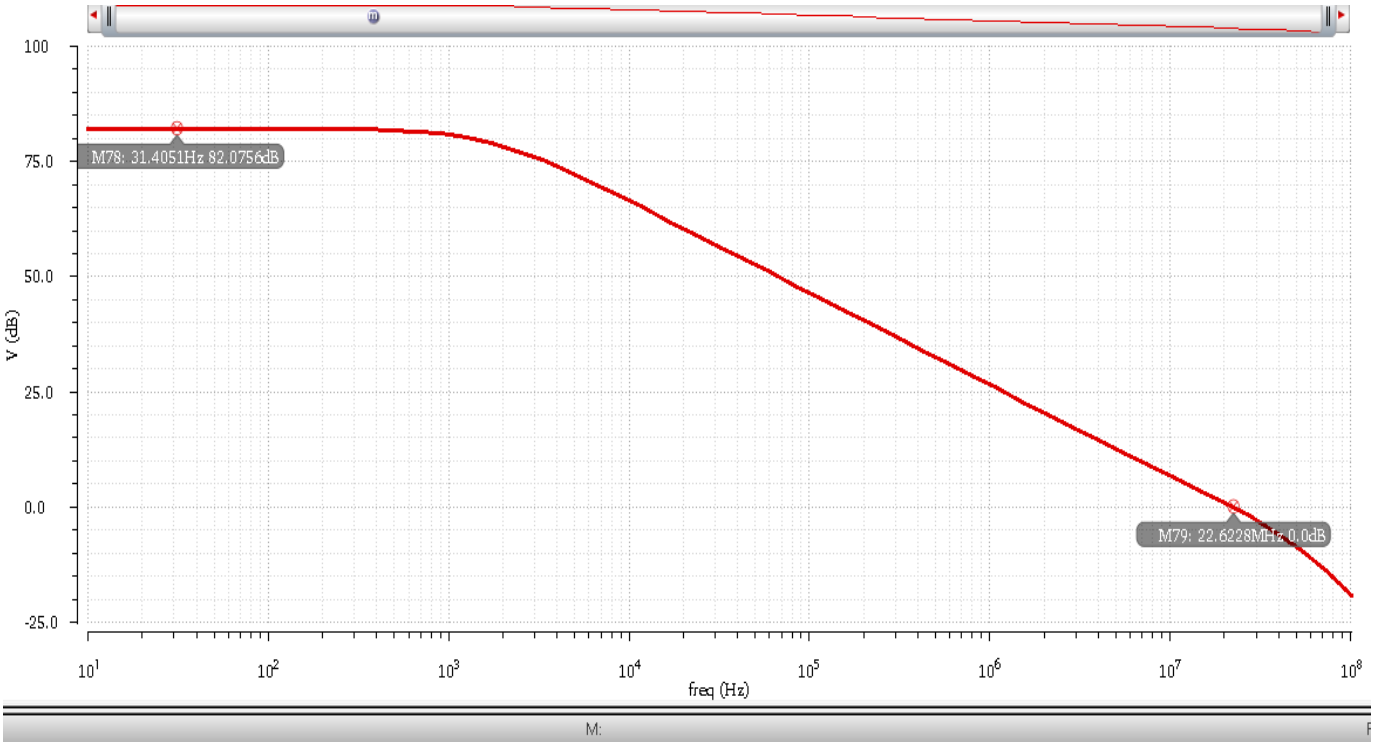

Figure 4: Gain in dB vs Frequency plot.

As shown in Figure 4, the graph of gain in dB vs frequency represents that the gain is of 82 dB at M78 mark and the unity gain frequency at 0dB is 22.6228 MHz at M79 mark. The unity gain frequency is also called as gain bandwidth product. The proposed result of gain is greater than 82% than the previous result [15].

As shown in Figure 5, the graph represents that the phase margin at mark M77 where the gain bandwidth product is 22.6228 Mhz comes to be 69^o that is remarkable for a 2-stage CMOS OpAmp to be stable. The previous result for phase margin was 60^o and now it is 69^o which is increased by 9^o, which is an increment of 15% from the previous value [15].

The power dissipation is the total amount of power that is consumed by the circuit. The power dissipation comes to be 219.6µW as shown in figure 6 which is quite low from previous result. The previous result of the parameter power dissipation was 271µW which is greater than the present result. The power dissipation is reduced by 19% from the previous result [15].

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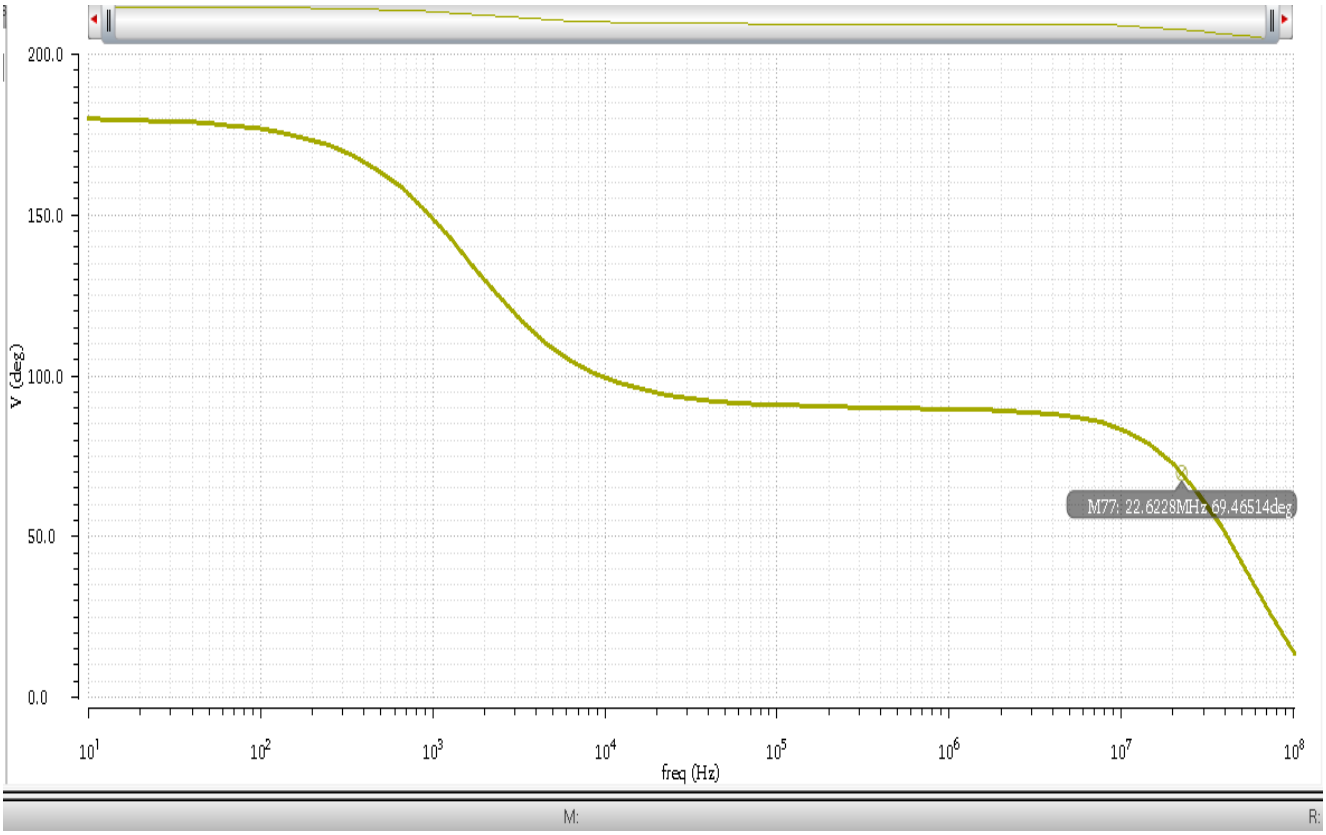

Figure 5: Phase vs Frequency Plot.

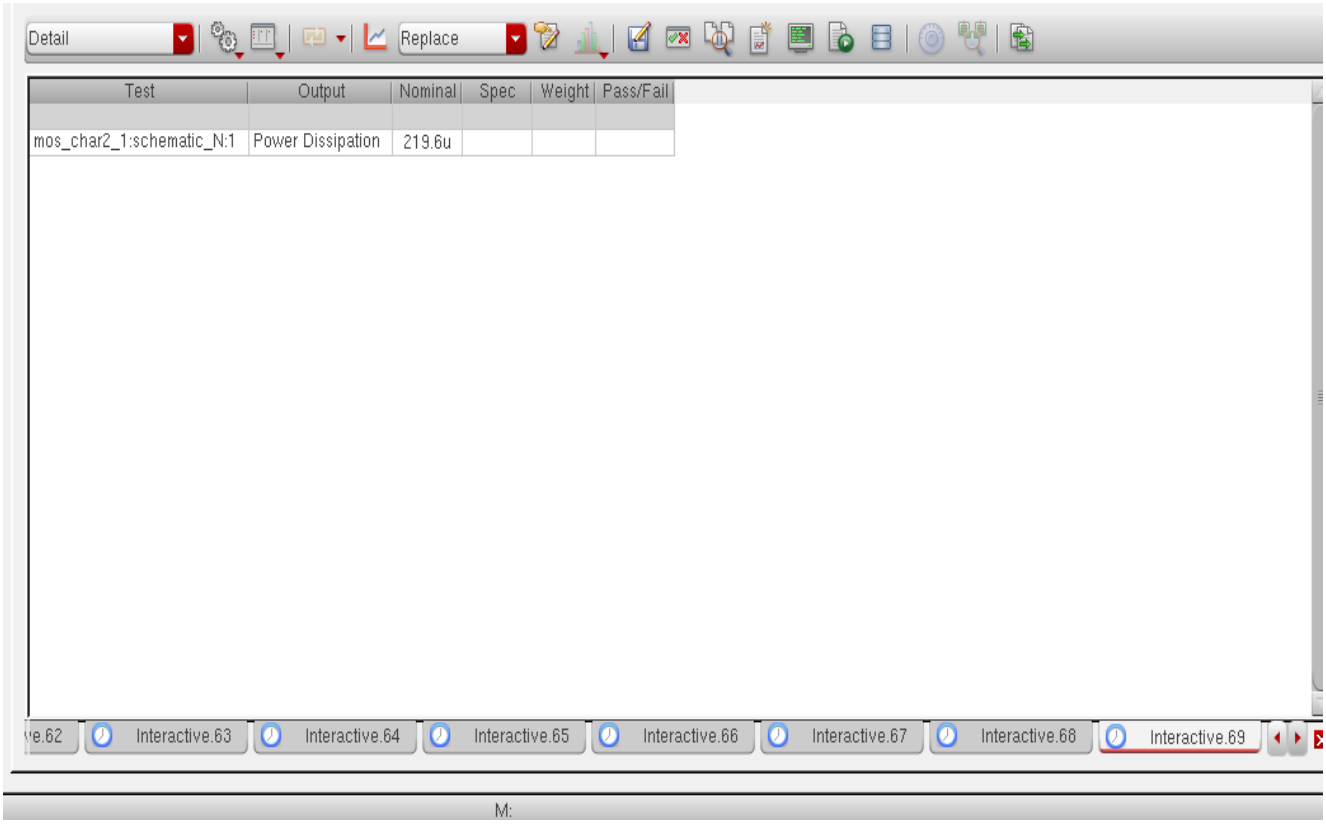

Figure 6: Power Dissipation Calculation.

Table 3: Comparison between previous and proposed result.

Parameters	Previous Results[15]	Proposed Results	Improvement
Gain	45 dB	82 dB	Increased by 82%
Phase Margin	60^o	69^o	Increased by 15%
Power Dissipation	271 µW	219 µW	Reduced by 19%
Unity Gain Frequency	25 MHz	22.6 MHz	Decreased by 2.4 MHz

Using 90 nm technology, after the simulation of 2 stage CMOS operational amplifier the results comes out on different parameters are much better than the previous results. As shown in table 3 the voltage gain margin is increased by 82%, phase margin is increased by 15%, power dissipation is reduced by 19% and unity gain frequency is decreased by 2.4MHz. Thus the operational amplifier stability is increased as phase margin increased, the gain is also increased and the power dissipation is reduced from previous result which makes the operational amplifier a stable, high gain and less power consumption amplifier.

5. CONCLUSION

As integrated circuit systems are created to appear as single-pole systems over a wide frequency range to reduce the problem that second order systems encounter with regard to stability, the simulation was performed using Cadence tool with 90nm technology. In order to achieve some design specification requirements, such as voltage gain and a better phase margin, Miller compensation technique is used. The gain has been improved by adjusting the parameters up to 82 dB. The circuit is appropriate for high performance, low power VLSI applications. The gain

bandwidth product result comes to be 22.6228 MHz. The power dissipation is of 219 µW and phase margin of 69° which makes the proposed operational amplifier suitable for low power operation with greater stability.

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