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A Speed Enhancing Technique for SAR Analog to Digital Conversion

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Abstract: High resolution analog to digital converters (ADCs) have been based on self-calibrated successive approximation (SAR) technique. Unfortunately SAR technique requires N comparisons to convert N bit digital code from an analog sample. This makes SAR ADCs unsuitable for high speed applications. Our proposed technique reduces number of comparison requirements to N/4 for N bit conversion. The main features of this paper are the efficient circuit configuration for SAR ADC. A new circuit configuration which requires N/4 comparisons for N bit conversion is presented. This technique increases conversion speed by 75%. Therefore this technique is best suitable when high speed combined with high resolution is required. An experimental prototype of proposed 16 bit ADC was implemented using Philips P89V51RD2BN Microcontroller. Use of Microcontroller has greatly reduced the hardware requirement and cost. The results show that the ADC exhibits a maximum differential nonlinearity (DNL) of 0.59LSB and a maximum integral nonlinearity (INL) of 0.58LSB.

Keywords: ADC, DAC, DNL, INL, Microcontroller, Sample and Hold, SAR.

1. INTRODUCTION

Digital audio applications require high resolution ADC with at least 16-bits or even more for a signal bandwidth of 20 kHz. Oversampled Σ - Δ convertors can achieve such a resolution at a reasonable cost [1]. A resolution of 16 bits has already been demonstrated with second-order mono-bit Σ - Δ loops with a sampling ratio of 256 [2]. Higher resolutions at a viable sampling frequency would require higher order modulator. However, these systems usually need extra circuit to cope with the potential instability of these loops [3]. An alternative is the use of self-calibrated SAR ADCs [4]. But this architecture is unsuitable for high speed applications. Two step flash converters are popular for conversion resolutions in the 8-12 bit range where optimized designs can achieve low power dissipation and small silicon area for implementation [5]. However, beyond such resolution, the area and power dissipation of two-step flash ADCs nearly double for each additional bit of resolution [6].

There are many different architectures like pipelined convertor [7], SAR convertor, Σ - Δ convertor; folding ADCs [8] reported recently for high speed applications. But these architectures have significant amount of complexity. In this paper a simple technique for enhancing conversion of SAR ADC is proposed.

2. FLASH ADC

Flash ADCs also known as parallel ADCs are the fastest way to convert an analog signal to a digital signal [9].

3. SAR ADC

SAR ADCs are widely used for high resolution 10-12 bit, medium speed 5MS/s, low-power, low-cost applications such as automotive, factory automation, and pen digitizer applications [10]. SAR ADCs with improved performance, lower cost, and higher reliability can make a significant impact in industry. A conventional SAR ADC consists of a track-hold circuit, comparator, DAC, SAR logic and time-base circuits [9].

4. PROPOSED ADC ARCHITECTURE

A wide variety of SAR ADC architectures have been described by several authors [1-3]. SAR ADCs are promising for low power, high resolution applications. However, high resolution limits the speed. The ADC based on our technique enjoys the benefit of employing only 22 comparators, while maintaining the advantage of high speed. In the proposed technique, segmentation process increases the speed of conversion. Block diagram of the 16 bit ADC using proposed technique is illustrated in Fig. 1. In the proposed technique, the analog input range is partitioned into 16 quantization cells, separated by 15 boundary points. A 4 bit binary code 0000 to 1111 is assigned to each cell. Where 4 bit flash ADC works as first stage which decides within which cell the analog sample lies and produces 4 bit binary code corresponding to that cell. It is the 4 MSB's of 16 bit digital code. Second stage as SAR ADC this produces remaining 12 LSB's of final 16 bit digital code.

The ADC consists of an input sample and hold amplifier (SHA), a 4 bit flash ADC, seven 16 bit DAC, 8-bit Microcontroller 8051, and some extra supporting circuit blocks. We propose an SAR ADC that has seven comparators and seven DAC for seven reference voltage outputs. These reference voltages will be as follows: V1 = (1/8)Vref, V2 = (1/4)Vref, V3 = (3/8) Vref, V4 = (1/2) Vref, V5 = (5/8) Vref, V6 = (3/4)Vref and V7 = (7/8)Vref. This ADC requires N/4 comparisons for N bit conversion. A conventional SAR ADC has only one comparator with reference voltage output VDAC = (1/2)Vref and hence it requires N comparisons for N-bit quantization.

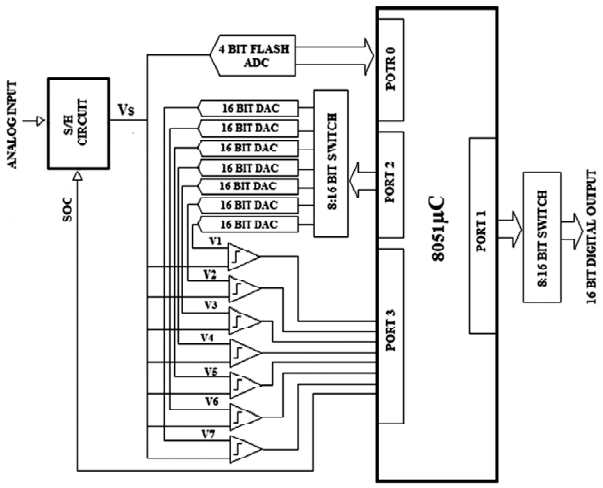

Figure 1: Block Diagram of 16 bit ADC

4.1. Circuit Implementation

The block diagram of the 16 bit ADC is as shown in Fig. 1. The microcontroller port 0 is used as input port, which gets the 4 bit code from 4 bit flash ADC, corresponding V1 to V7 reference voltage 16 bit binary code of a particular cell is loaded into the accumulator and R0. Port 2 is used as output port and it is connected to seven 16 bit DACs through 8:16 bit MUX/DMUX switch to obtain seven reference voltages V1 to V7 of particular cell. These voltages are compared with an analog input voltage Vs. Equivalent 12 LSBs for analog input signal is obtained by SAR technique. The conversion algorithm is similar to the binary search algorithm. First, the reference voltages V1 to V7 provided by DAC's are set to (1/8) Vref , (1/4)Vref, (3/8)Vref, (1/2) Vref , (5/8)Vref, (3/4)Vref and (7/8)Vref of particular cell to obtain the first three bits, values of three bits depends upon comparator outputs. If all three comparator outs V1 to V7 are 1, then values are 111. If comparator outs are 1111110, then values are 110. If comparator outs are 0000000, then values are 000. After getting three bits, SAR convertor moves to the next three bits .This sequence will continue until the last three LSBs are obtained. In every comparison three bits are obtained. To get an 12 LSBs, 4 comparisons are needed. Finally 16 bit digital code is available at 8:16 bit MUX/DMUX switch through port 1.

Software for implementing SAR converter in Microcontroller is written in assembler code and converted to hex code by assembler software. Hex codes are transferred to microcontroller by programmer.

5. RESULT AND DISCUSSION

An experimental prototype of 16 bit ADC using proposed technique was designed and developed using Philips P89V51RD2BN. The working functionality of the ADC has been checked by generating a ramp input going from 0 to 5V (full scale range of the ADC). Digital codes have been obtained correctly, going from 0 to 65536 for 16 bits at the output, indicating that the ADCs working is functionally correct.

Both the DNL and INL were measured over 2^{16} output codes by applying slowly varying full scale range ramp as input to the proposed ADC, which completes the full scale range in 65536 steps. The values of the each code are compared with ideal value and store the difference value. The results show that the ADC exhibits a maximum DNL of 0.52 LSB and a maximum INL of 0.55LSB as shown in the Fig. 2(a) and 2(b).

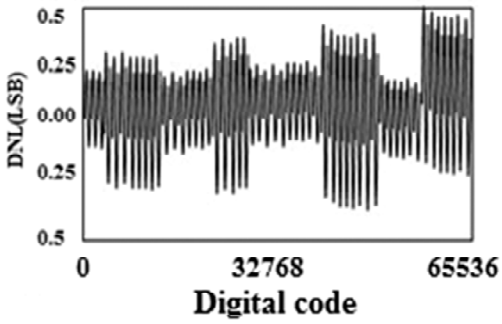

Figure 2(a): Differential Non Linearity

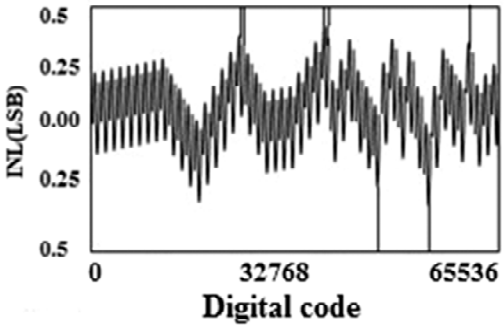

Figure 2(b): Integral Non Linearity

6. CONCLUSION

We have designed and developed a high-performance SAR ADC architecture that achieves both high speed and high reliability - ideal for automotive, high speed controls and signal processing applications such as hard-disk-drive read channel wireless receivers and digital audio applications etc. ADC results of 16bit prototype are presented. Implementation

of SAR algorithm in Microcontroller has reduced the hardware requirement and cost. We further plan to implement this architecture and algorithm efficiently on an IC.

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