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# An Ancient Indian Mathematics Based Multiplier: SADHNA

(**Systematically Acting Device Helping in Numerical Analysis**)

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**Abstract-** A multiplier is widely used in digital signal processing such as in filters and in computer hardware design. It is generally needed in carrying out complex computations and as such affects the devices' performance in terms of speed, cost, flexibility, on- chip area, etc. Thus, to design a multiplier with best possible efficiency in terms of speed, cost, on- chip area, etc. is the need of the day. In this paper an attempt has been made to design a multiplier based on ancient Indian mathematics (Vedic Mathematics). It has been designed using Xilinx ISE 8.2i. The coding has been done in VHDL and the FPGA used is QProVirtexE Military xqv600e-6-bg432.
**Keywords-**Multiplier, Adder, Urdhva-Tiryagbhyam, Entity, SADHNA.

## 1. Introduction

This paper embodies following objectives:

A To study the unconventional method of multiplication given in the Indian Vedas.
B To design a multiplier structure based on our study of the ancient method of multiplication.
C To synthesize and simulate the designed multiplier.
D To generate test bench for the designed multiplier.

## 2. Literature review

### A. Origin of the Idea

The work, Vedic Mathematics or the 'Sixteen Simple Mathematical Formulae from the Vedas', was written by His Holiness JagadguruSankaracharya Sri BhartiKrisnaTirthaji Maharaja of GovardhanaMatha, Puri (1884 - 1960). It forms a class by itself not pragmatically conceived and worked out as in the case of other scientific works, but is the result of the intuitional visualisation of fundamental mathematical truths and principles.
This paper is based on the literature cited from a part of a Parisista of the Atharvaveda. Each Veda has its subsidiary apocryphal texts some of which remain in manuscripts and others have been printed but that formulation has not closed. For example, some parisistas of the Atharvaveda were edited by G.M. Bolling and J. Von Negelein, Leipzig, 1909-10.

### B. Problem with the Conventional Method

This method is mathematically correct, but it has two serious engineering problems. The first is that it involves 32 intermediate additions in a 32-bit computer, or 64 intermediate additions in a 64-bit computer. These additions take a lot of time. The engineering implementation of binary multiplication consists, really, of taking a very simple mathematical process and complicating it a lot, in order to do fewer additions; a modern processor can multiply two 64-bit numbers with 16 additions (rather than 64), and can do several steps in parallel—but at a cost of making the process almost unreadable. The second problem is that the conventional method handles the sign with a separate rule ("+ with + yields +", "+ with - yields -", etc.). Modern computers embed the sign of the number in the number itself, usually in the two's complement representation. That forces the multiplication process to be adapted to handle two's complement numbers, and that complicates the process a bit more. Similarly, processors that use one'scomplement, sign-and-magnitude, IEEE-754 or other binary representations require specific adjustments to the multiplication process.

## 3. In detail paper

A **Conventional Multiplication**

Suppose we multiply 12 by 13 using conventional method of multiplication, then it will be done as given below:

$$\begin{array}{r} 12 \\ \times\ 13 \\ \hline 36 \\ +\ 12X \\ \hline 156 \\ \hline \end{array}$$

Thus we see that by using the conventional method of multiplication even a two digit by two digit multiplication becomes so tedious as it takes so many steps to reach the final answer. This means that if such a multiplication algorithm be applied for multiplication in the computers then it will take many second to perform even a small multiplication thus, for processes requiring multiplications all the time will take hours to execute.

**B.MultiplicationByUrdhva - Tiryak Sutra**

Urdhva- Tiryagbhyam Sutra is the general formula applicable to all cases of multiplication and is also very useful in the division of a large number by another large number. This formula itself is very short and terse, consisting of only one compound word and means "vertically and cross-wise". The applications of this brief and terse sutra are manifold.

**C. Modus Operandi**

A simple example with suffice to clarify the modus operandi thereof.
Suppose we have to multiply 12 by 13.

$$\begin{array}{r} 12 \\ \times\ 13 \\ \hline 1\text{: } 3 + 2\text{: } 6 = 156 \\ \hline \end{array}$$

Steps carried out:

- We multiply the left - hand – most digit one of the multiplicand vertically by the left hand most digit one of the multiplier, get their product one and set it down as the left hand most part of the answers.
- We then multiply one and three, and one and two crosswise, at the two, get five as the sum and set it down as the middle part of the answer; and
- We multiply two and three vertically, get six as their product and put it down as the last right hand most part of the answer. Thus, 12 multiplied by 13 is equal to 156.

**D. Algebric Principle Invovled**

Suppose we have to multiply (ax+b) by (cx+d). The product is $acx^2+ x (ad + bc)$. In other words the first term such that the coefficient of $x^2$ is got by vertical multiplication of a and c. The middle term such that the coefficient of x is obtained by the cross wise multiplication of a and d and of b and c and the addition of the two products; and the independent term is arrived by vertical multiplication of the absolute term. And, as all arithmetical numbers are merely algebraic expressions in x (with x=10). The algebraic principle explained above is readily applicable to arithmetic numbers too. Now if our multiplicand and multiplier is of 3 digits each, it merely means that we are multiplying $(ax^2 + bx + c)$ by $(dx^2 +ex + f)$.

- That the coefficient of $x^4$ is got by the vertical multiplication of the first digit from the left side;
- That the coefficient of $x^3$ is got by the cross wise multiplication of the first two digits and by the addition of the two products;
- That the coefficient of $x^2$ is obtained by the multiplication of the first digit of the multiplicand by the last digit of the multiplier, of the middle one by the middle one and the last one by the first one and by the addition of all the three products;
- That the coefficient of x is obtained by the cross wise multiplication of the second digit by the third one and conversely by the addition of the two products;
- That the independent term results from the vertical multiplication of the last digit by the last digit.

We thus follow a process of accent and of decent going forward with the digits on the upper row and coming rearward with the digits on the lower row.

### E. Program Development

The design is based on mixed modeling which has been done using component instantiation. Component instantiation is done for four components as explained below:-

- First component configured is a two input multiplier with integer range (-2147483647 to 2147483647).
- Second component configured is a two input adder with integer range (-2147483647 to 2147483647).
- Third component configured is a three input adder with integer range (-2147483647 to 2147483647).
- Fourth component configured is four input adder with integer range (-2147483647 to 2147483647).

### F. Software Implementation

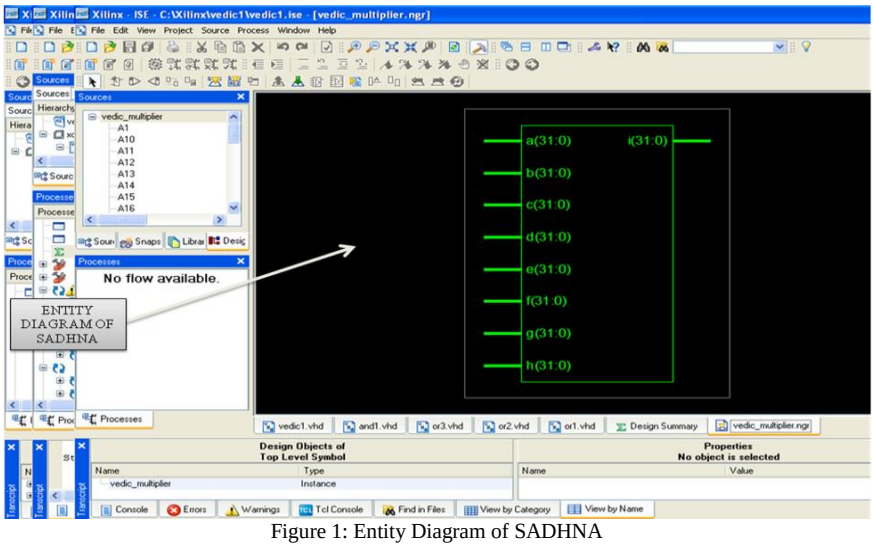


Figure 1: Entity Diagram of SADHNA

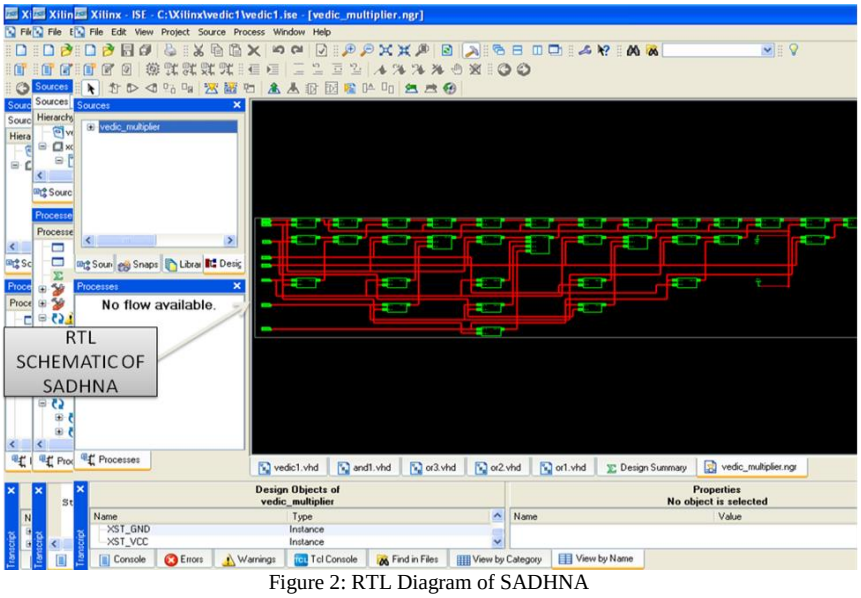


Figure 2: RTL Diagram of SADHNA

### G. Test Bench Waveform

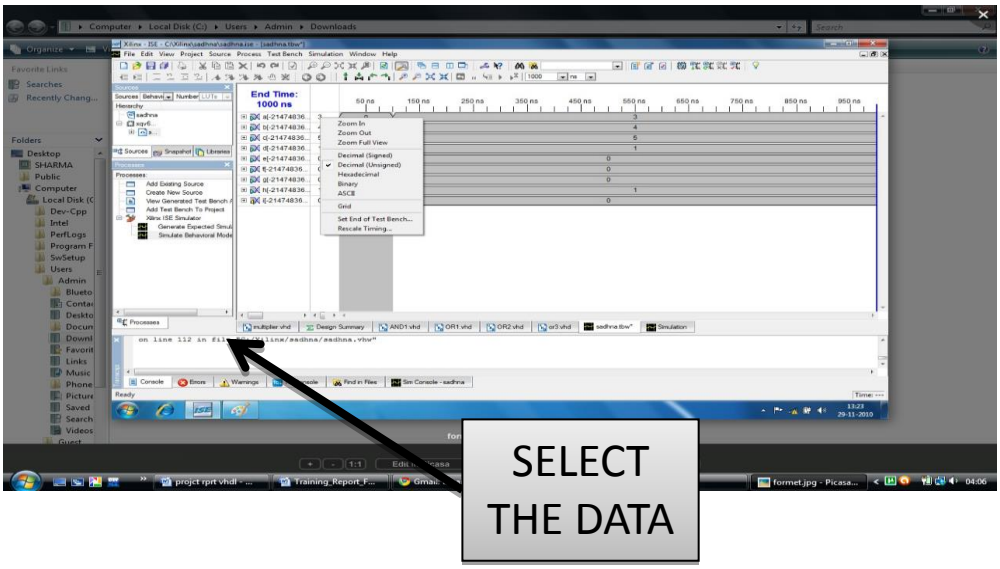


Fig 3: Selecting the Data

**H. Final Design Summary**

The design summary sums up the project status, partition summary, device utilization summary and the detailed reports.

From the device utilization summary we come to know that 60% of the total available slices were used, 58% of the total available 4 input look up tables (LUTs) were used and 86% of the total available bonded input outputs (IOBs) were used.

## 4. CONCLUSION

Multipliers are widely used in the digital signal processing and in computer hardware design, especially in the digital filters. In realization of large order filters speed, cost and flexibility is affected because of complex computations but this can be minimized by the use of a very efficient multiplier. Thus, multipliers with best possible efficiency in terms of speed, cost and chip area utilized is the need of the day.

In this paper a 4X4 multiplier named SADHNA (Systematically Acting Device Helping in Numerical Analysis) based on the ancient Indian mathematics was coded in VHDL, designed using Xilinx ISE8.2i and implemented on QProVirtexEMillitary xqv600e-6-bg432.

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