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Comparative Analysis of Low-Power OTA Operating In Weak Inversion Region

ReetuRani[1] ,Kuldeep Singh[2]
[1]M.Tech Student
[1]Department of Electronics and Communication Engineering, Guru Jambheswar University Science and Technology, Hissar (Haryana)
[1]Rbansal41@gmail.com, [2]Kuldeep.elect@gmail.com

ABSTRACT - In this paper comparative analysis of two realization techniques of low-power ,low-voltage fully differential CMOS OTA is presented. The circuits are biased in weak inversion. The study encompasses slew rate , power dissipation , bias current and delay . Analysis has been done in mentor graphics with TSMC .35µm , .25µm , .18µm technology .
Keywords: OTA , Folded OTA , Power dissipation , Slew Rate

I. INTRODUCTION

The OTA is a basic building block in most of analogue circuit with linear input-output characteristics. The OTA is widely used in analogue circuit such as neural networks, Instrumentation amplifier, ADC and Filter circuit [4]. In most of the modern high performance analog integrated circuit is needed since it can extend the dynamic range over one order of magnitude through cancellation of even harmonic, as well as suppression of undesirable common mode signals. Some of the key attractive properties of OTA are their fast speed in comparison with conventional low output impedance op-amps and their bias dependence transconductance tunability [6].
The transistors are traditionally biased in the saturation mode in analogue circuits. But, they can be operated in strong inversion or weak inversion.Transistors biasing in weak inversion provide higher transconductance and supply a larger gain with a smaller current. These transistors present a low thermal noise [3]. The features of this technique are higher voltage gain , lower device power consumption , higher output resistance. The topologies analyzed here are FD-OTA and folded cascode OTA , both biased in weak inversion.

A. Operation of MOS device in weak inversion region:

In weak inversion where the source is tied to bulk , the current varies exponentially with V_{GS} as given by (1)

$$I_D = I_{D0} e^{\frac{V_{GS}-V_{th}}{nV_T}} \qquad (1)$$

Where I_{D0} is the current at $V_{GS} = V_{th}$ (threshold voltage) , V_T is thermal voltage (about 25 mV at room temperature) and n is the slope factor.

II. Basic Concept of FD-OTA

The circuit symbol of the FD-OTA (fully differential operational transconductance amplifier) is given in Figure 1a.

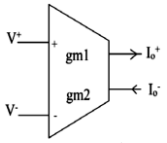

Figure 1. Symbol of FD-OTA

Ideally, dual output OTA is assumed as an ideal voltage controlled current source. It has infinite input and output impedances. The output current can be expressed as (2)

$$I_{0-} = I_{0+} = g_m(V_1 - V_2) \qquad (2)$$

Where g_m is the transconductance of FD-OTA .
In case of weak inversion mode g_m can be expressed as (3)
$g_m = \frac{I_B}{2nV_T}$ (3)

$$I_0 = g_m \frac{I_B}{2nV_T} \quad (4)$$

$$I_0 = g_m V_{in} \quad (5)$$

Where V_T , n , $I_B$are the thermal voltage , subthreshold slope and the input bias current respectively.
Generally, the transconductances of the dual output OTAs are chosen as $g_{m1} = g_{m2}$ similar to the topologies described in this work. For some applications unequal $g_{m1} = g_{m2}$values are obtained by taking different width and length values for MOS transistors of the output stages.

A. Circuit Configuration

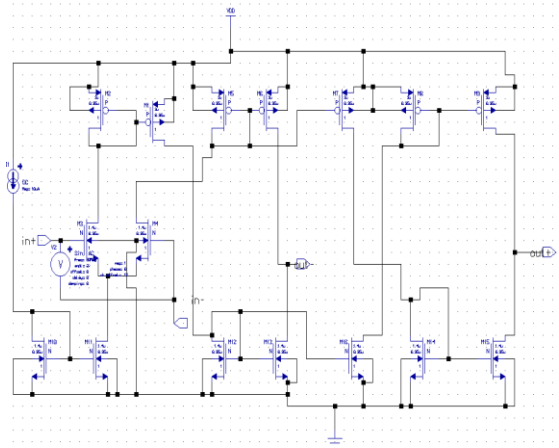

Figure 2. FD-OTA

From fig. 2, M_3 andM_4 works as conventional differential pair input and all other transistor pair works as simple current mirror. We can also use other topologies for current mirror to enhance the performance.

III. FOLDED CASCODE OTA

A MOS cascode is a common-source common-gate amplifier. In folded cascode CS is N channel type and CG is P channel type that will reverse the direction of signal flow back toward ground. Its main advantages are high output impedances , increased output swing , reduction in unwanted capacitive feedback in amplifier and high gain.
As shown in fig. 3. It has a input differential input stage consisting of NMOS transistor $M_1$and M_2, M_5 and M_{12} provide the DC bias voltage to M_3,M_4 ,M_{10} ,M_{11} .

Open loop voltage gain (A_v)=$\frac{g_{m2} \cdot g_{m8} \cdot g_{m6}}{I_D^2 (g_{m6} \lambda_N^2 + g_{m8} \lambda_P^2)}$ (6)

Where, g_{m2}, g_{m6} , g_{m8} are respectively the transconductance of M_2 , M_6 andM_8 respectively. $I_D$is the bias current. $\lambda_N$andλ_P are the parameters related to channel length modulation.

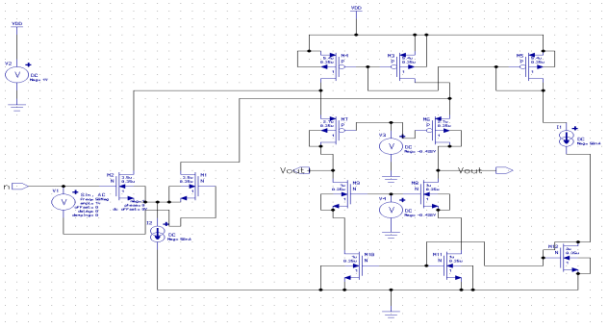

Figure 3. Folded OTA

IV. SIMULATION RESULTS

Simulation has been done in mentor graphics with TSMC .35µm , .25µm , .18µm technology at different frequencies with a supply voltage of .8V for FD-OTA and 1V for Folded OTA. Bias current is varied from 10µA-100µA for FD-OTA and 10nA-50nA for Folded OTA.

Fig. 4 and fig. 5 shows the transient response of FD-OTA and Folded OTA with a sinusoidal signal of frequency 250MHz with Ibias= 50µA and 30nA respectively.

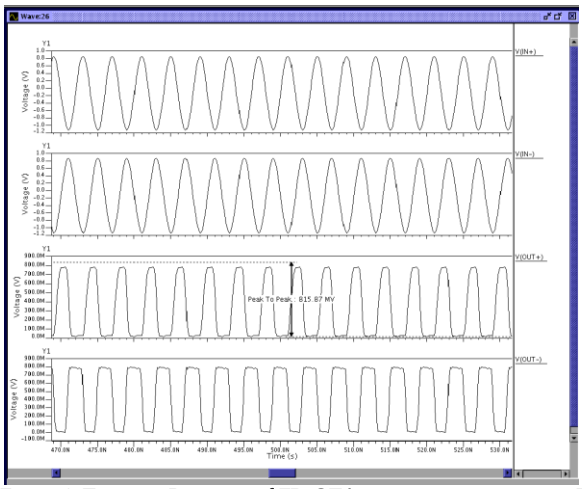

Figure 4: Transient Response of FD-OTA

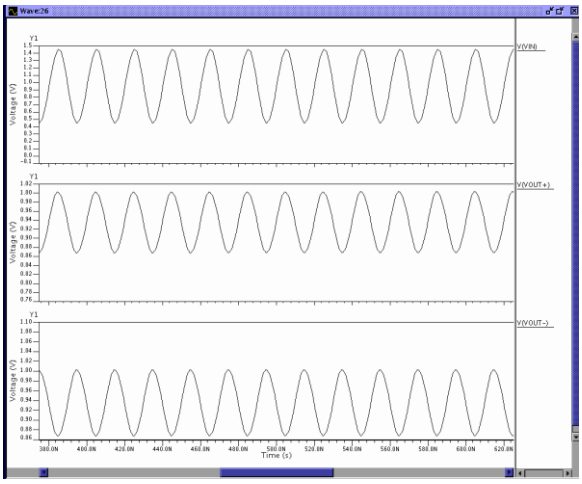

Figure 5: Transient Response of Folded OTA

Table1:

FD OTA (TSMC350nm)		FOLDED OTA (TSMC350nm)	
Ibias=10µA		Ibias = 10nA	
PD(µW)	Freq. (MHz)	PD(µW)	Freq. (MHz)
7.4596	800	22.8646	800
7.4596	500	22.8646	500
7.4596	250	22.8646	250
Ibias= 25µA		Ibias= 20nA	
PD(µW)	Freq. (MHz)	PD(nW)	Freq. (MHz)
21.3344	800	47.2827	800
21.3344	500	47.2827	500
21.3344	250	47.2827	250
Ibias=50µA		Ibias=30nA	
PD(µW)	Freq. (MHz)	PD(nW)	Freq. (MHz)
49.3263	800	72.3062	800
49.3263	500	72.3062	500
49.3263	250	72.3062	250
Ibias= 75 µA		Ibias=40 nA	
PD(µW)	Freq. (MHz)	PD(nW)	Freq. (MHz)
82.4672	800	97.7289	800
82.4672	500	97.7289	500
82.4672	250	97.7289	250
Ibias=100 µA		Ibias=50 nA	
PD(µW)	Freq. (MHz)	PD(nW)	Freq. (MHz)
120.2499	800	123.4519	800
120.2499	500	123.4519	500
120.2499	250	123.4519	250

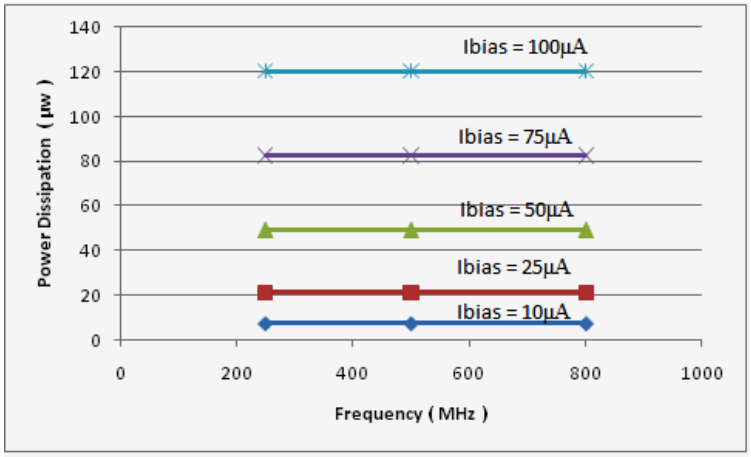

Figure 6: Plot of Power dissipation Vs Frequency at Different values of Ibiasfor FD-OTA

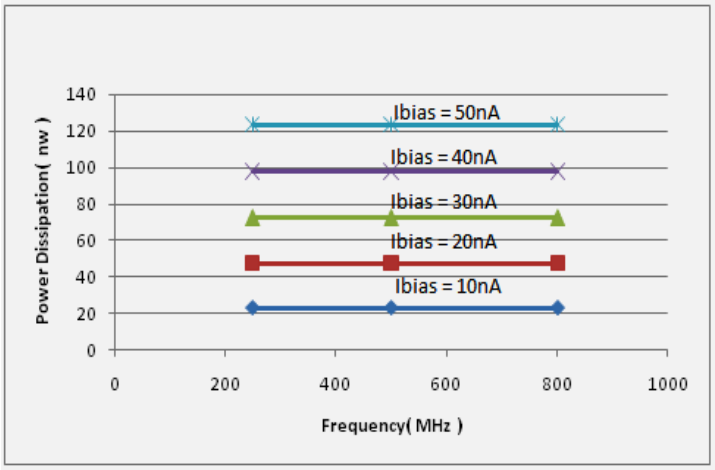

Figure 7: Plot of Power Dissipation Vs Frequency at Different values of Ibiasfor Folded - OTA

As shown by plots for weak inversion biased OTA power dissipation increase with increase in Ibias but change in frequency does not affect power dissipation.

Table2:

Frequency (MHz)	PD (µW) 350nm	PD (µW) 250nm	PD (µW) 180nm
800	49.3263	37.8412	34.7001
500	49.3263	37.8412	34.7001
250	49.3263	37.8412	34.7001

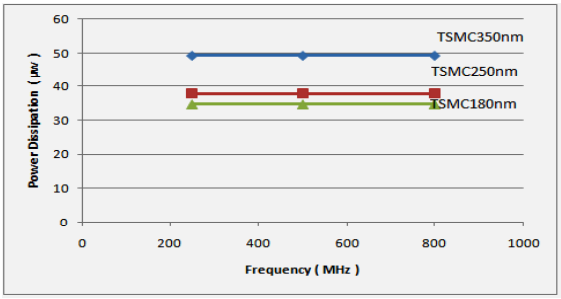

Figure 8: Plot of Power Dissipation Vs Frequency at Different Technologies for FD-OTA (Ibias=50µA)

Table 3:

Frequency (MHz)	PD (nW) 350nm	PD (nW) 250nm	PD (nW) 180nm
800	72.3062	56.2233	54.2536
500	72.3062	56.2233	54.2536
250	72.3062	56.2233	54.2536

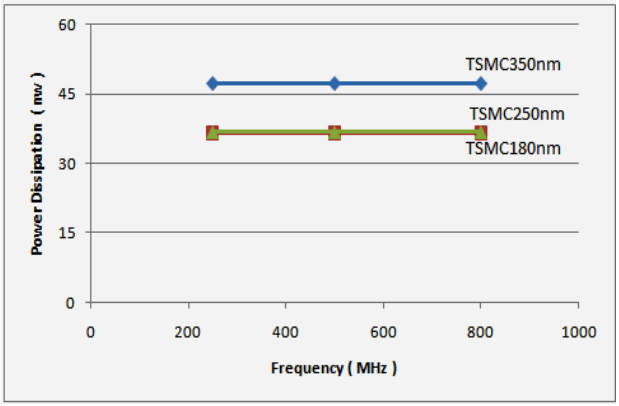

Figure 9: Plot of Power Dissipation Vs Frequency at Different Technologies for Folded-OTA (Ibias=30nA)

It is obvious from fig. 8 and 9 that increase in feature size tends to increase the power dissipation of both OTAs.

Table 4:

Frequency (MHz)	Delay 1 (350nm)	Delay 2 (250nm)	Delay 3 (180nm)
800	1048	178.64	292.47
500	1337.4	922.35	663.37
250	2422.3	2217.8	2630.8

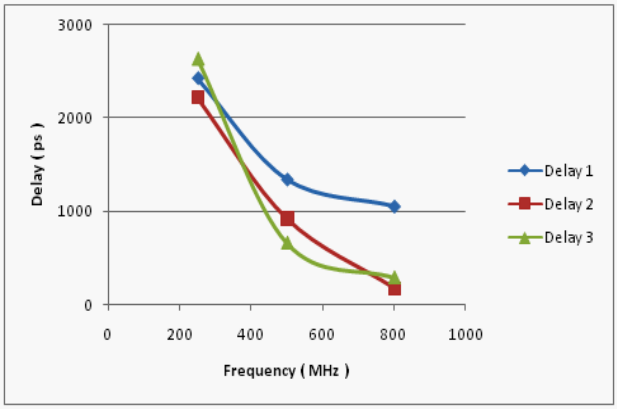

Figure 10: Plot of Delay Vs Frequency at Different Technologies for FD-OTA (Ibias=50µA)

Table 5:

Frequency (MHz)	Delay 1 (350nm)	Delay 2 (250nm)	Delay 3 (180nm)
800	198.99	2416.1	1093.5
500	1851.7	1900.2	1792.3
250	3606.4	3927.9	3710.3

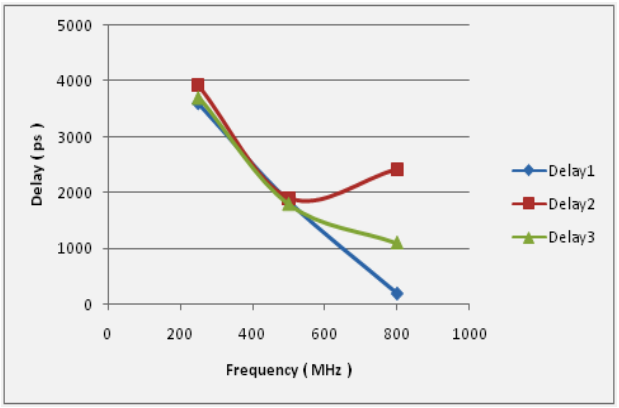

Figure 11: Plot of Delay Vs Frequency at Different Technologies for Folded-OTA (Ibias=30nA)

Fig. 10 and 11 shows that delay decrease with decrease of feature size and increase of frequency.

Table 6:

Frequency (MHz)	Slew Rate1 (350nm)	Slew Rate2 (250nm)	Slew Rate3 (180nm)
800	437.45	352.7	495.45
500	147.69	386.56	907.14
250	200.74	1234.5	2352.6

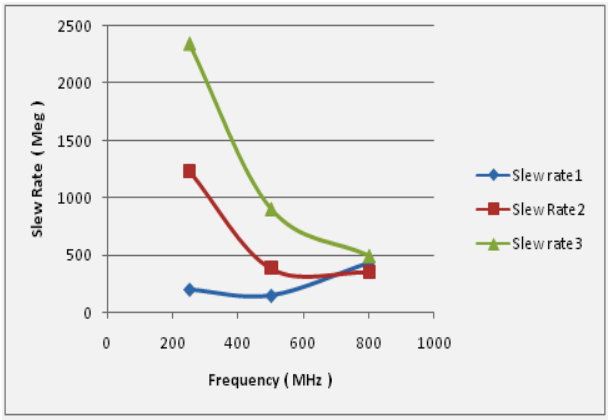

Figure 12: Plot of Slew Rate Vs Frequency at Different Technologies for FD-OTA (Ibias=50µA)

Table 7:

Frequency (MHz)	Slew Rate1 (350nm)	Slew Rate2 (250nm)	Slew Rate3 (180nm)
800	291.26	290.52	445.61
500	150.52	175.08	264.99
250	80.224	78.111	122.48

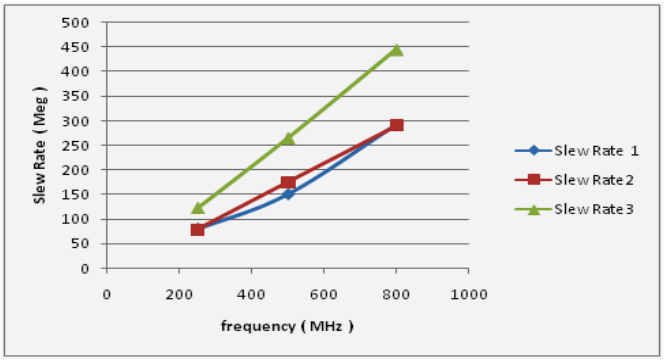

Figure 13: Plot of Slew Rate Vs Frequency at Different Technologies for Folded-OTA (Ibias=30nA)

Slew Rate of FD-OTA decrease with increase of frequency but for folded-OTA it increase with increase of frequency.
Technology have same impact on Slew Rate for both circuits.

V. CONCLUSION

Aim of this study is to analyze OTA circuits that can work efficiently in weak inversion region. For low voltage operation these circuits are suitable. FD-OTA has power dissipation of the order of µW and for Folded-OTA it is of the order of nW.Future work would involve exploitation of these results to design a low power phase ADC .

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