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ANALYSIS AND DESIGN OF Z-RAM FOR LOW LEAKAGE CURRENT

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In this paper, the analysis and design of Zero-Capacitor Random Access Memory (ZRAM) cell for low leakage current have been done. The ZRAM cell is a special type of DRAM cell based on bipolar transistor present in the MOSFET, designed by using SOI (Silicon on Insulator) Technology. The transistor used in the ZRAM is 0.5µm SOI n-MOSFET. For the analysis, fully depleted SOI n-MOSFET (ZRAM) and partially depleted SOI n-MOSFET (1T-DRAM) have been considered. Process simulation and device simulation of SOI based ZRAM cell and 1T-DRAM cell have been carried out using the ATHENA/ATLAS packages of SILVACO TCAD tool. ATHENA software is used for generating the structure of ZRAM cell and then it is used as input to device simulator ATLAS for its electrical characterization. It has been shown that ZRAM having fully depleted SOI n-MOSFET has lower leakage current than 1T-DRAM cell (Partially depleted SOI n-MOSFET). Leakage reduction from 2.26nA to 1.03nA in the device has been achieved successfully

Keywords: Z-RAM (FDSOI n-MOSFET), Bipolar Transistor, 1T-DRAM (PDSOI n-MOSFET), Floating Body Effect

1. Introduction

In order to reduce manufacturing cost, power and leakage current of DRAM, which consists of one transistor and one capacitor (1T/1C), for large capacity and high speed, the memory cell has to be scaled down continuously. However, it requires a complicated stack capacitor or a deep –trench capacitor in order to obtain a sufficient storage capacitance (around 30fF/cell) in smaller cells. It can't be scaled below 100nm. Also in DRAM cell due to the presence of capacitor, the current reduces and after few seconds there is need of refreshing the data stored in the cell. In order to overcome the effect of leakage current a capacitor-less 1T-DRAM cell has been investigated as an alternative solution [1-2]. It uses a floating -body of a partially depleted (PD) silicon on Insulator (SOI) MOSFET as a storage node. The new concept of Zero-capacitor DRAM (ZRAM) based on bipolar transistor present in the MOSFET also known as fully depleted (FD) SOI MOSFET, has been reported and exhibited low power, high speed, and improved data retention time [3] and was recently further confirmed[4]. Innovative Silicon, Inc. (ISi), a memory technology company founded in 2002, is the inventor and licensor of the Z-RAM®. These earlier publications do not show the exact leakage current in ZRAM cell. In this paper 1T-DRAM cell (PDSOI n-MOSFET) and ZRAM (FDSOI n-MOSFET) are considered for the analysis and proved that ZRAM cell has lower leakage current than 1T-DRAM cell.

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2. The SOI MOSFET

A cross-section view of a proposed structure of SOI MOSFET is shown in Fig. 1. Depending on the film thickness (t_{si}) and doping in the silicon film, the SOI MOSFETs fall into categories: PDSOI MOSFET and FDSOI MOSFET. When the silicon film is thick, only the top portion of the film is depleted and the bottom portion is neutral. There will be no interaction between the front and the back gates. This type of SOI MOSFET is called PDSOI MOSFET or 1T-DRAM. However, when the neutral region is grounded the PDSOI MOSFET will behave very much like the bulk MOSFET with same equations and design concepts. If the body is not connected, the device will have floating body effects that are undesirable to circuits operations. If the silicon film is thin such that the entire film will be depleted, a FDSOI MOSFET i.e. ZRAM will be obtained. In this case there will be interaction between the front and the back gate leading to a good coupling.

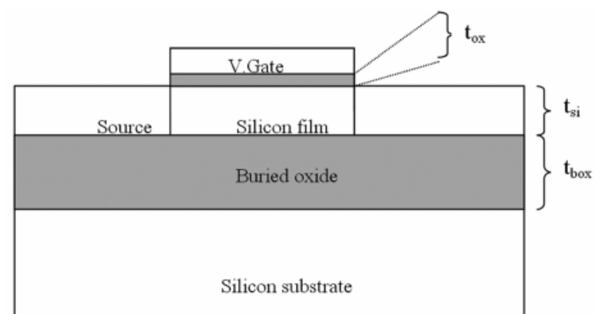

Fig. 1: Cross Sectional View of an SOI nMOSFET

3. Device Simulations

Simulations of fully depleted 0.5μm SOI n-MOSFET (silicon film thickness=90nm) and partially depleted 0.5μm SOI n-MOSFET (silicon film thickness=150nm) were performed by the SILVACO TCAD tools [5-6]. Typical values of the various transistor parameters used in these simulations are shown in Table 1.

Table1
Process Parameters for the Design of 0.5 SOI n-MOSFET

Parameter	Symbol	Unit	Value
SOI Film Thickness (PDSOI)	Tsi	nm	150
Silicon film thickness (FDSOI)	Tsi	nm	90
Starting SOI Film Resistivity	–	Ω-cm	p-type, 14
Substrate concentration (Boron)	–	cm^3	1×10^{15}
Channel doping (Boron)	–	cm^3	1.7×10^{17}
N-type polysilicon doping	–	cm^3	1×10^{20}
Gate length	Lg	μm	0.5
Buried Oxide Thickness	T_{BOX}	nm	400
Gate Oxide Thickness	T_{OX}	nm	15
N+ Poly Gate Thickness	T_{Poly}	nm	200
Threshold Voltage	V_{th}	nV	300

For process simulation an initial substrate mesh is defined. It is consisting of the silicon substrate, the buried oxide layer and the silicon thin film. A finer mesh should exist in those areas of the simulation structure where ion implantation will occur, where p-n junction will be formed. The buried oxide has a thickness of 0.4μm and the silicon thin film thickness is 90 nm in FDSOI n-MOSFET (ZRAM) and 150nm in PDSOI n-MOSFET (1T-DRAM). The substrate and the thin film were initially doped with boron (p-type) of concentration $1X10^{15}$ cm^{-3}. The boron implantation is performed to set the doping 1evel in the substrate. A thin oxide is then grown on the SOI wafer and a nitride layer is deposited. Chemical etching of nitride and oxide is carried out to form p- well. After etching process wet oxide is diffused and then etches all nitride. Next Boron is implanted in the p-well to adjust threshold voltage. The gate is an n-type polisilicon doped with $1 \times 10^{20}cm^{-3}$ of phosphorus atoms. The device's gate length can be changed during the polysilicon-etching step. For simulating a short channel device, an LDD source/drain will overcome the hot carrier effects. The LDD source /drain is formed be using phosphorus while heavily doped source/drain is formed by using arsenic. The threshold voltage, leakage current and gate oxide thickness is extracted during run time. Fig. 2 (a) and 2(b) shows the simulated 0.5 μm FDSOI n- MOSFET (ZRAM) and 0.5 μm PDSOI n- MOSFET (1T-DRAM) respectively.

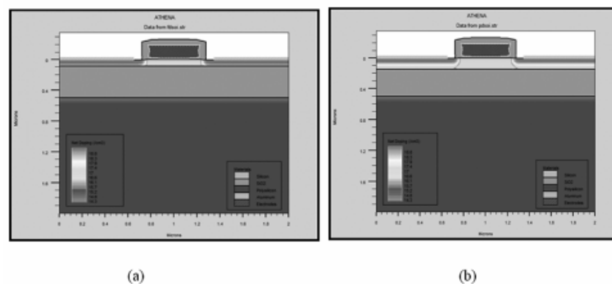

Fig. 2: (a) Structure of FDSOI n-MOSFET (ZRAM)
(b) PDSOI n-MOSFET (1-T DRAM)

4. Simulation Result and Discussion

Process simulation of ZRAM cell and 1T-DRAM cell has been carried out using the ATHENA packages of SILVACO and then it is used as input to device simulator ATLAS for its electrical characterization. With device simulation, the effect of process parameters and its variation on the electrical characteristics of ZRAM cell (FDSOI SOI nMOSFET) and 1T-DRAM (PDSOI nMOSFET) is studied.

4.1 The combine Id – V_{gs} Characteristics for ZRAM and 1T-DRAM with gate length = 0.5μm, gate oxide length = .015μm, Buried oxide thickness = 0.4 μm at Vds = 0.1V.

From figure 4.1 it is observed that the threshold voltage of ZRAM (FDSOI n-MOSFET) is 0.45V and 1T-DRAM (PDSOI n-MOSFET) is 0.55V. It means that with the decrease of thickness of silicon film (Tsi) the threshold voltage decreases and hence increases leakage current, but by increasing channel length of ZRAM, threshold voltage is increased and hence leakage current is improved. The run time leakage current output is 1.03nA in ZRAM cell and 2.23 nA in case of 1T-DRAM cell at Vgs = 0V and Vds = 0.1V.

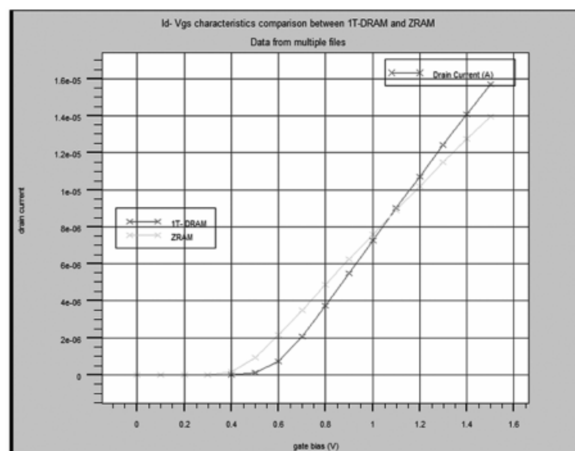

Fig. 4.1: Combine Simulated Id-Vgs Characteristics for ZRAM and 1T-DRAM

4.2 Combine subthreshold characteristics of 1T-DRAM cell and ZRAM cell at Vds = 0.1V.

From figure 4.2 it is observed that subthreshold slope of 68 mV/decade is in ZRAM and 88 mV/decade in 1T-DRAM at Vds = 0.1V. The subthreshold leakage is reduced as the silicon film is made thinner.

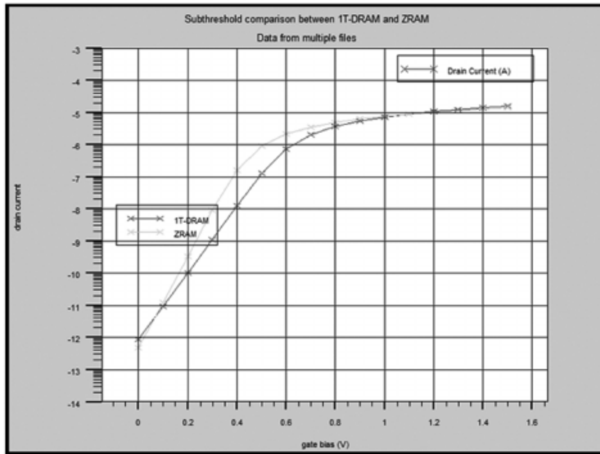

Fig. 4.2: Combine Subthreshold Characteristics for 0.5 μm ZRAM and 1T-DRAM at Constant Value of Vds = 0.1V. Note that y-axis is in Log Scale

4.3. The Id–Vds Characteristics

The combine I_d-Vds characteristics at constant value of Vgs= 1.5V for ZRAM and 1T-DRAM is given in figure 4.3. It shows that kink effect is present in 1T-DRAM cell and there is no kink in ZRAM cell.

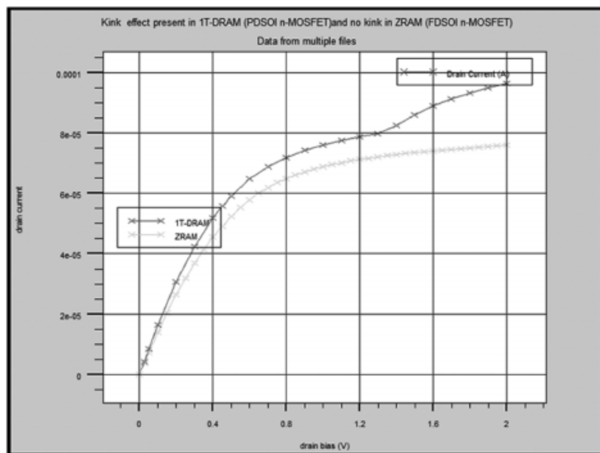

Fig. 4.3: Combine Id-Vds Characteristics for a 0.5 μm 1T-DRAM Cell and ZRAM Cell at Constant Gate Voltage = 1.5V. Kink Effect Present in 1T-DRAM But Eliminated in ZRAM

In ZRAM (FDSOI n-MOSFET), the leakage current in the junction is negligible in static mode. Irrespective of what value the cell is storing, no holes accumulate in the body to increase the body potential. The reason for this is that the source body potential barrier is very low in FDSOI n-MOSFET and all holes injected will easily be swept into the source without increasing the body potential. As a result of this, even when bit line voltage i.e. gate voltage changes, there will be no diffusion mechanisms as in 1T-DRAM (PDSOI n-MOSFET) to discharge the storage capacitor. Thus ZRAM provides the longest retention time and reduces leakage current. The performance of the ZRAM cell is evaluated in this section. Table 2 summarizes the simulation results and the comparison with 1T-DRAM cell.

Table 2
Simulated Device Performance of a PDSOI n-MOSFET (1T DRAM Cell) and FDSOI N-MOSFET (ZRAM Cell)

Parameter	Unit	PDSOI n-MOSFET (1T-DRAM)	FDSOI n-MOSFET (ZRAM)
SOI Film Thickness (Tsi)	nm	150	90
Gate Oxide hickness (Tsi)	nm	15	20
Gate Length	μm	0.5	0.52
Threshold Voltage (V_{th})	mV	0.55	0.45
Subthreshold Slope (S)	mV/decade	88	68
Leakage Current	nA	2.26	1.03
Kink in the output	–	Yes	No
Ids(Vds=0.8V,Vgs-th) =1.0V	mA/mm	42	46

5. Conclusion and Future Scope

The characteristics of Z-RAM cell (FDSOI n-MOSFET) and 1T-DRAM cell (PDSOI n-MOSFET) using 0.5μm technology node are presented. It is concluded that ZRAM cell (FDSOI n-MOSFET) has lower leakage current of 1.03 nA than 1T-DRAM cell (PD SOI n-MOSFET) of 2.26nA. The leakage current is inversely proportional to the threshold voltage and channel length. The threshold voltage in 1T-DRAM is more than that of ZRAM but, by increasing channel length in ZRAM it is improved and hence leakage current is also reduced. High drain voltage improves threshold voltage and leakage current but it increases power. The main drawback in 1T-DRAM cell is kink effect, which is eliminated in ZRAM. The Z-RAM cell is demonstrated to be a promising technology for embedded memories.

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